1988

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Brian R. Khabbaz
Lehigh University

MMIC DESIGN, ANALYSIS AND LAYOUT FOR A 6-10 GHz SERRODYNE PHASE SHIFTER AND A LINEAR DOUBLE BALANCED MESFET MIXER

by

R. Brian Khabbaz

A Thesis

Presented to the Graduate Committee

of Lehigh University

in Candidacy for the degree of

Master of Science

In

Electrical Engineering

Lehigh University

1988

This thesis is accepted and approved in partial fullfillment of the requirements for the degree of Master of Science.

May 17, 1988
(Date)

D. Richard Decker
Professor in charge

L. J. Vannoni
Chairman of Department

ACKNOWLEDGEMENTS

I would like to thank professor D. R. Decker for his guidance and support throughout this thesis and the rest of my graduate studies at Lehigh University. I would also like to thank the graduate students I have been associated with in the past two years. Finally I thank my family for their moral support.

This thesis is dedicated to Donna.

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Abstract

The design, analysis and mask layout have been performed for two MMICs. The first MMIC is a 6-10 GHz serrodyne phase shifter. The second is a linear double balanced MESFET mixer. The analysis and mask layouts were done using the facilities at Lehigh University and will be fabricated by a foundry. A description of the design, operation, analysis and mask layout of the two MMICs will follow. The CAD tools used and foundry interaction so the MMICs can be fabricated will be discussed.

INTRODUCTION

Gallium arsenide monolithic microwave integrated circuits (MMICs) are microwave circuits which have all the active and passive circuit elements and interconnections formed into the bulk of a semi-insulating GaAs substrate. MMICs provide many advantages over their hybrid MIC counterparts. MMICs require extensive CAD modeling [1]. This is due mainly to the effects of coupling at high frequencies. A general procedure for designing MMICs that has been used in this thesis will be oulined next.

The procedure used to design these circuits is outlined in figure 1. The first step is to develop a concept you would like to implement monolithically. The second step is to design the circuit using microwave devices and circuit elements. These devices include IMPATT diodes, Schottky barrier diodes, MESFETs and HEMTs. When designing MMICs one must keep in mind that the values of resistors, capacitors and inductors must be realistic. If the element values are smaller than the technology allows they simply can't be built and if the elements are too large they will take a excessive amount of space. The next step is the simulation and optimization.

The simulation tools used for MMICs are discussed in

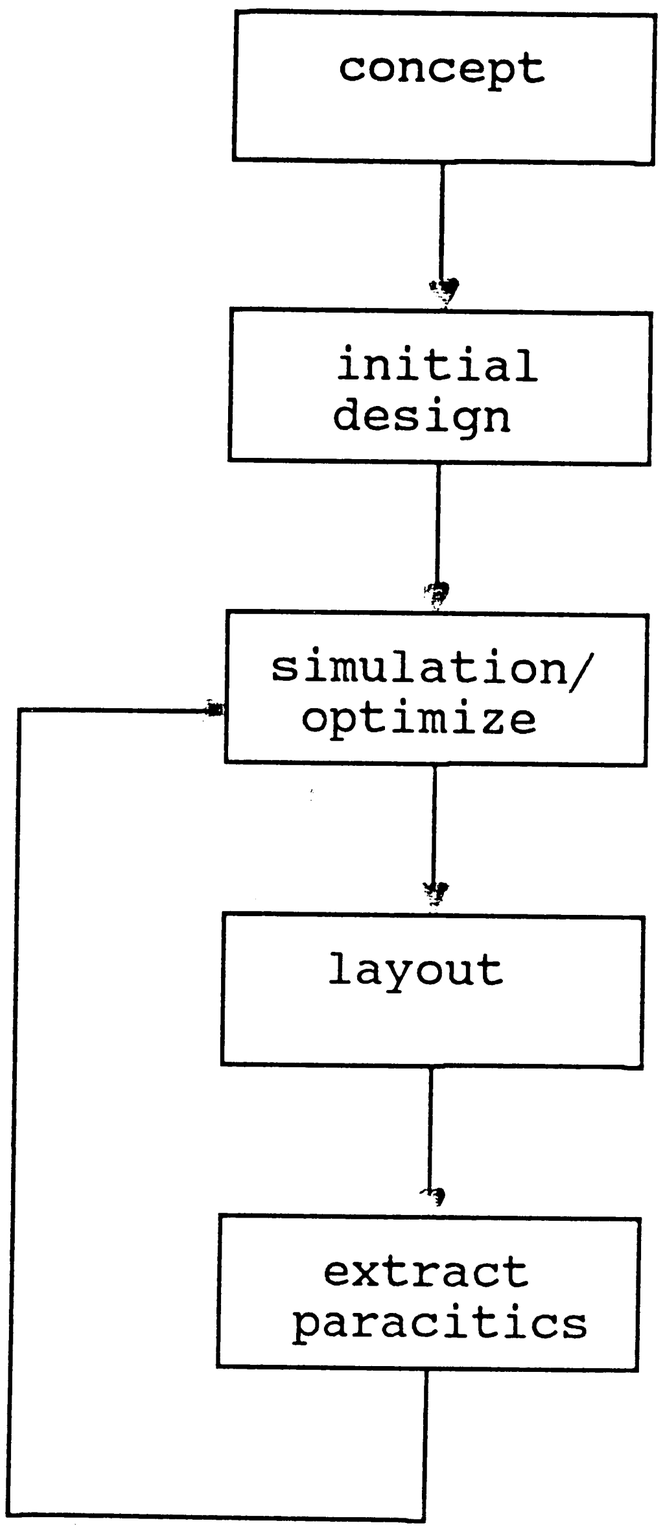

concept
initial design
simulation/ optimize
layout
extract paracitics

Fig. 1

the next section. The step after the simulation and optimization is the mask layout. The mask layout is done with the help of a set of design rules from the foundry that will do the fabrication. When the layout is complete, the parasitics must be extracted and used to resimulate the circuit. This is one of the crucial parts of the design because the physical layout may have considerable differences from the ideal circuit. Extracting all the parasitics, taking the coupling into consideration, and modeling the transmission lines correctly is where the extensive modeling and design interaction come into play.

The procedure above was the procedure used in this thesis. The simulation tools, circuit operation and performance, and layout will be discussed in the following sections.

SIMULATION TOOLS

Circuit simulators are used to get an accurate idea of the behavior of a circuit before it is fabricated. The two general types of simulation tools used for the analysis of circuits are the linear, small signal analysis, and the nonlinear large signal analysis. These simulators will be discussed in general.

General

The circuit simulators from the University of California, Berkeley, SPICE sells for a small fee to cover the cost of shipping and handling. Many other software companies have circuit simulators, however they add visual graphics which make the software more attractive and charge a price much higher than Berkeley. These circuit simulators can simulate DC, AC and transient solutions of the circuit. Also included in these packages is a GaAs MESFET model which can be used for analysis of microwave circuits.

SPICE 3a7, Berkeley's latest version, contains the Statz et al. model [2] for the GaAs MESFET. This model is more accurate than the previous Curtice model used in SPICE. In particular, the gate-to-source and gate-to-drain capacitances are more accurate in the Statz model. Berkeley's latest version of SPICE was used, alond with

PSPICE by Microsim Corp., to do the simulation for the MMICs in this thesis.

Linear Small Signal Analysis

A linear circuit simulator is the S parameter analysis. This type of analysis is used for microwave circuit simulation, especially microwave amplifiers. From the S parameter analysis one can quickly obtain the expected gain or the reflection coefficients of the input and output due to the mismatch of the source and load, respectively. The S parameter simulators available from companies like Super Compact can take measured S parameters of a FET and determine an equivalent circuit. The equivalent circuit can then be used to form a frequency dependent Z, Y, S, or cascade matrix as desired. With these matrix representations one can obtain a matrix representation for the entire circuit by cascading the component cascade matricies together. From the total cascade matrix we can then obtain any of the matricies mentioned above; for example, we can obtain the total S parameter matrix for the circuit. As mentioned above the total S parameter matrix will tell us the gain and the reflection coefficients.

Nonlinear Large Signal Analysis

The nonlinear analysis is used for large-signal applications. One large signal application of interest is the analysis of mixers. Most software available, from the software companies, is for the nonlinear analysis of diodes in mixer applications. Many theorists have been working on nonlinear FET models [3] and FET mixer programs [4] so we can expect the software companies to advertise FET mixers analysis programs shortly.

The nonlinear problem can be solved by the standard harmonic balance technique. This is an iterative technique which seeks to match the frequency components(harmonics) of the current in a set of branches joining two subcircuits [5]. The linear part or embedding network, is solved in the frequency domain and the nonlinear part, the diode or FET, is solved in the time domain. These two solutions must be matched at each point and each time step in order for the solution to exist. Figure 2 shows a mixer with its linear embedding network and its nonlinear diode separated for the analysis.

Limitations of Simulators

As mentioned before, Berkeley's latest version of SPICE along with Microsim's version were used to do the analysis of the two MMICs designed in this thesis. Microsim's version worked well for the simulations, however

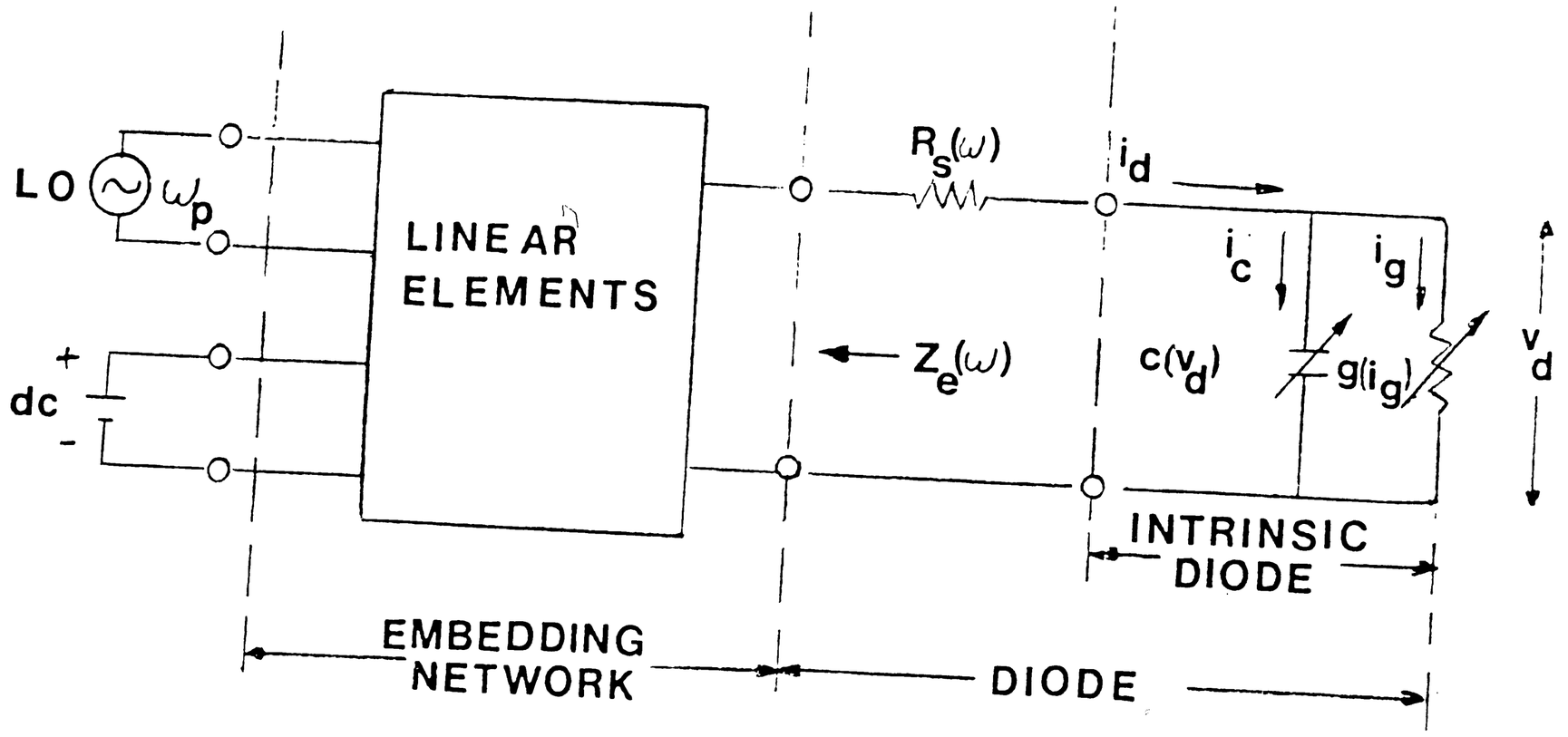

LO
ω_p
+
dc
-
LINEAR ELEMENTS
$R_s(\omega)$
$Z_e(\omega)$
i_d
i_c
i_g
$c(v_d)$
$g(i_g)$
v_d
INTRINSIC DIODE
EMBEDDING NETWORK
DIODE

Fig. 2

the MESFET model in this version is the Curtice model. Since Berkeley's version had the new Statz model, the circuits were also simulated with Berkeley's program. It was found that the Statz model was implemented in such a way that the drain current is a function of the absolute value of the drain to source voltage. This means that the derivative of drain current with respect to drain to source voltage is discontinuous. Since the time domain analysis is done by integrating the state equation, the time will not converge for the case when the drain to source potential goes from positive to negative because the state equation will be discontinuous. The DC analysis when using the Statz model also has some problems. The DC analysis does not converge as well as the Curtice model. This may be due to the form of the equation.

This problem of convergence with the Statz model was encountered in the analysis of the serrodyne phase shifter and the linear double balanced mixer. Each circuit requires the drain to source potential of a FET to go from positive to negative. The phase shifter has FETs used as variable resistors which will switch drain-to-source bias while in operation. The mixer is made of four GaAs MESFETs which will have to go from positive to negative drain-source bias. Each simulator has its advantages and disadvantages. Both simulators were used where they worked

for the specific application. The Curtice model was used for determining DC biases and when simulating the FETs where the drain-source bias switched potentials. The Statz model was used when predicting gain and wherever else possible for the DC, AC, and transient analyses. Both simulators were used to obtain the most accurate prediction of the circuit performance.

SERRODYNE PHASE SHIFTER

Basic Operation

The basic operation of a phase shifting circuit is to change the phase of the output signal relative to the input signal to achieve has some desired shift in phase. The serrodyne phase shifter is designed to operate from 6GHz to 10GHz. Any phase between 0 and 360 degrees can be obtained. In addition the phase can be varied continuously. This continuous phase change will actually give a frequency shift. This continuous change in phase, or frequency shift, is the meaning of the title "serrodyne". Figure 3 shows a block diagram of the serrodyne phase shifter.

The circuit has been designed using allpass networks and differential amplifiers to obtain four quadrature signals. After the quadrature signals are determined, MESFETs are used as variable resistance modulators. There are two differential amplifiers which have the quadrature signals on the four outputs. Between the outputs of each differential amplifier there are two MESFETs in series. These MESFETs have gate potentials 180 degrees out of phase so that one FET is on while the other FET is off. The point between the series FETs for each differential amplifier is then fed into an output differential amplifier. The circuit schematic illustration of the serrodyne phase shifter is shown in figure 4.

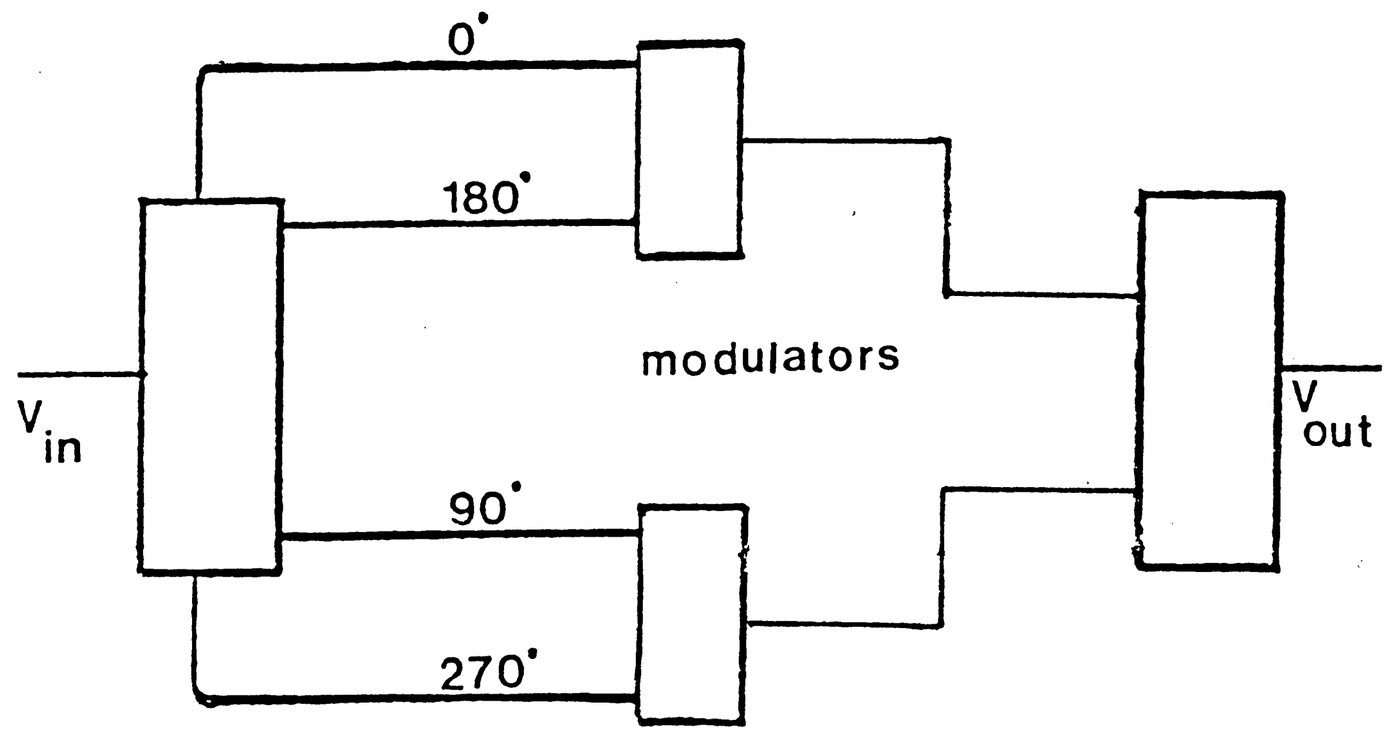


Fig. 3

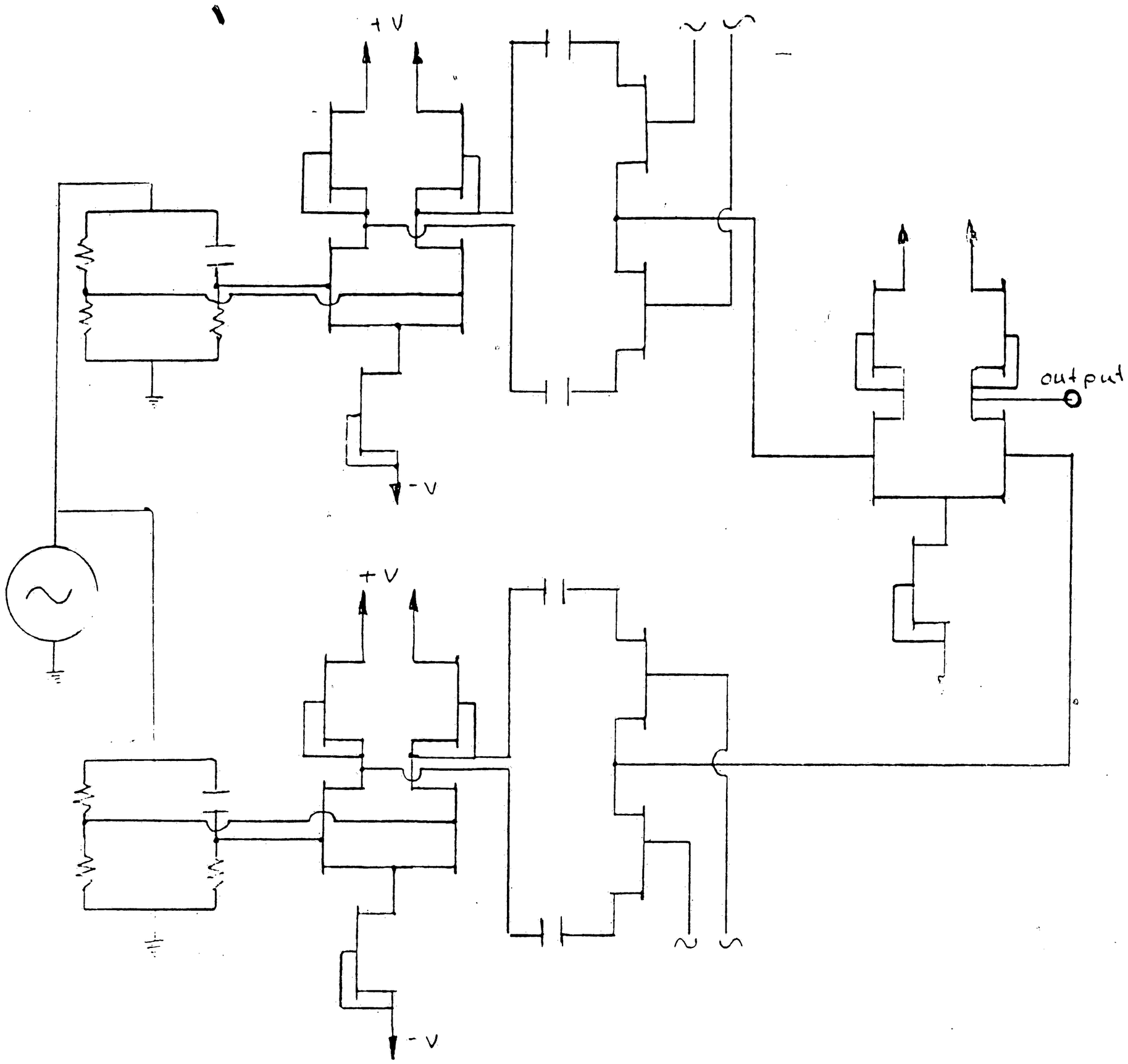


Fig. 4

Operation in Detail

The first problem faced was to obtain the four quadrature signals. This problem was solved with allpass filters which are RC circuits with three resistors and one capacitor shown in figure 5. This circuit was easily implemented monolithically. The magnitude and phase characteristics are shown in figure 6 a and b. Figure 7 shows a PSPICE simulation of the magnitude and phase characteristics. The output voltage can be taken differentially as can be seen in figures 4 and 5. The way in which we establish quadrature phases is to have two allpass networks which have different RC constants such that the phase difference is 90 degrees at the center of the band, 8GHz. Appendix A shows how to determine the values of capacitance to obtain quadrature signals. Appendix B lists a basic program which shows that we can maintain this phase relationship from 6 to 10 GHz. The 90 degree phase shift stays constant over the frequency range, 6 to 10 GHz, with variations of only one or two degrees at the band edges. Also, this bandwidth can be increased by adding poles and zeros to the transfer function of the allpass networks.

By taking the output from the allpass filters differentially with two differential amplifiers we can obtain the four quadrature signals. Each differential

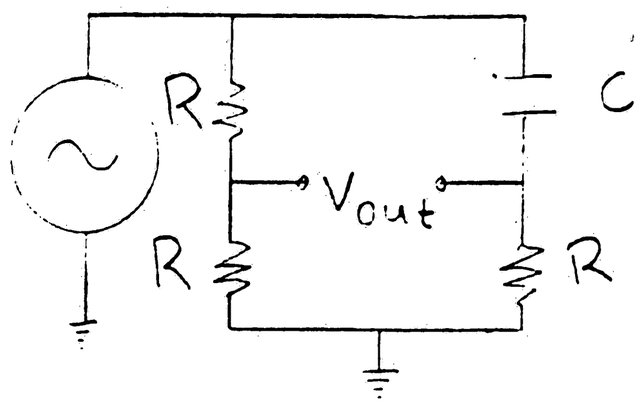


Fig. 5

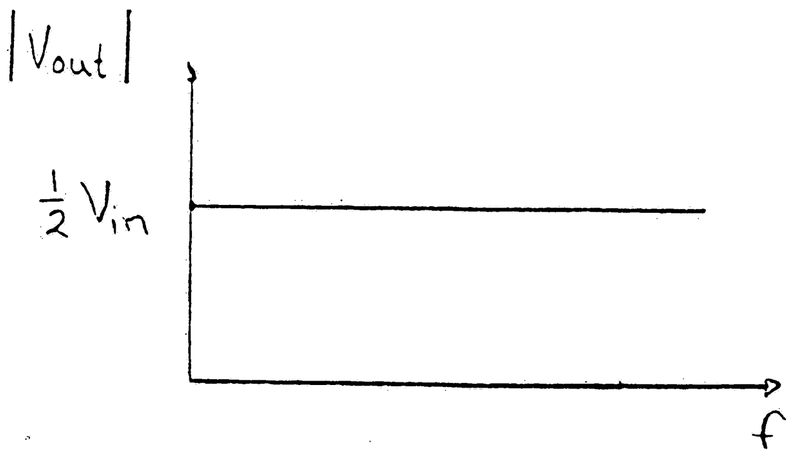


Fig. 6a

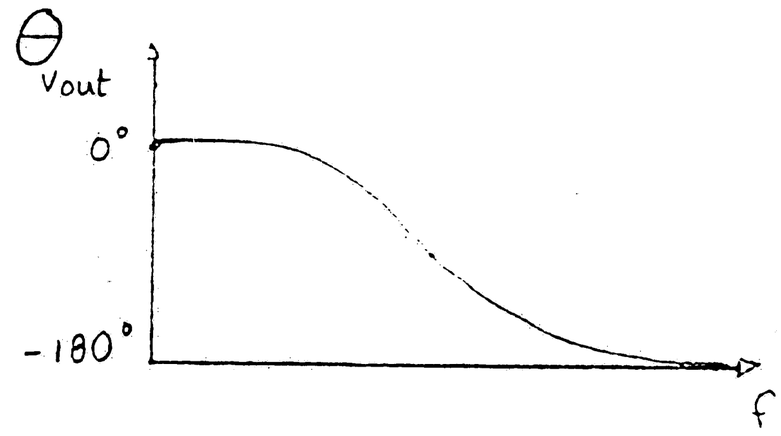


Fig. 6b

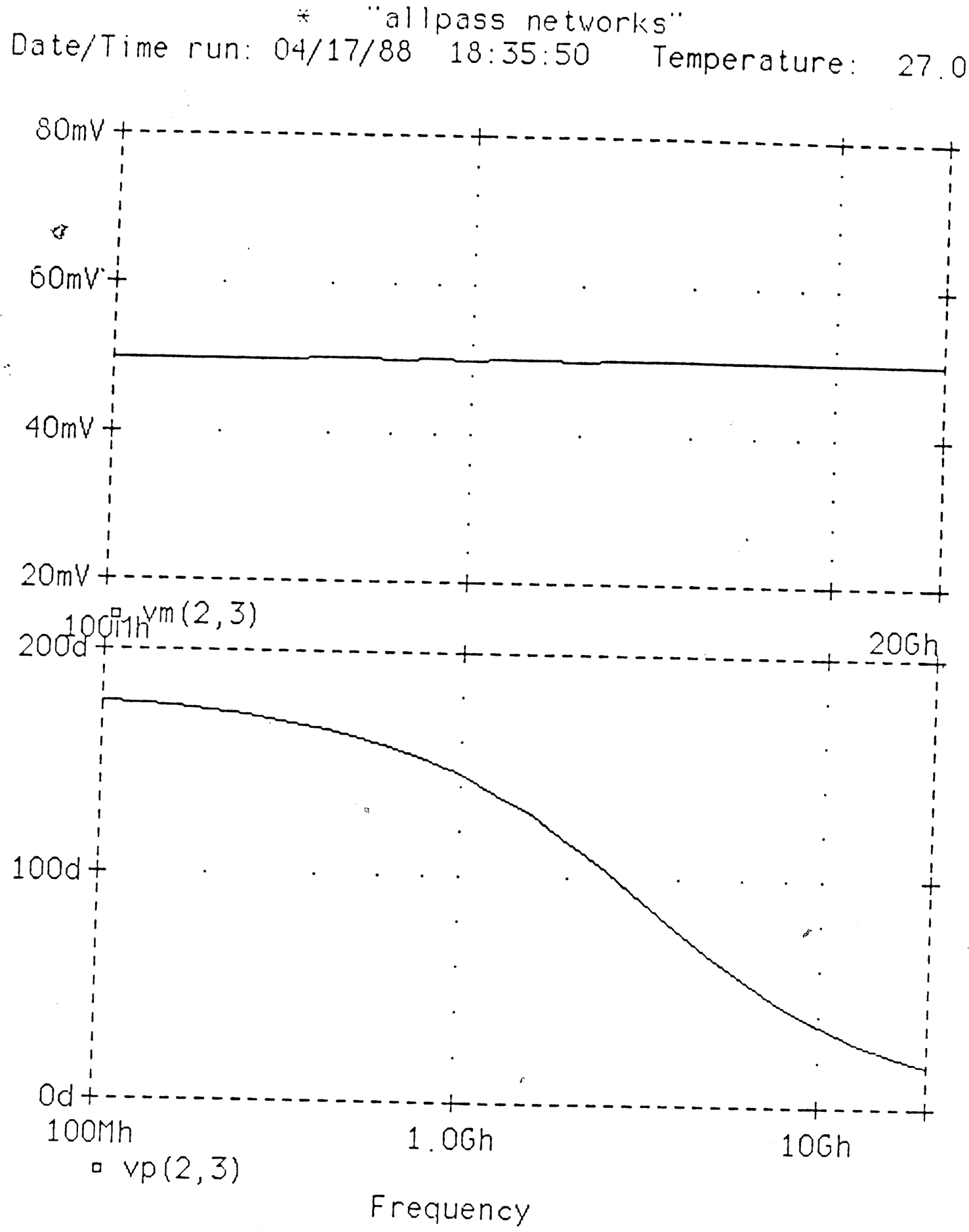

* "allpass networks"
Date/Time run: 04/17/88 18:35:50 Temperature: 27.0
80mV
60mV
40mV
20mV
100Mh
200d
100d
0d
100Mh
1.0Gh
10Gh
20Gh
vm(2,3)
vp(2,3)
Frequency

Fig. 7

amplifier has two outputs which are 180 degrees apart as shown in figure 8. Also shown in figure 8 are the saturated loads used for high gain. Since the inputs to the two differential amplifiers are 90 degrees out of phase we obtain the quadrature signals on the four outputs as shown in figure 9. The phase characteristics for the quadrature signals are shown in figure 10 from a simulation. Figure 11 illustrates the desired phase characteristics over the 6GHz to 10GHz band.

Once the quadrature signals are obtained, shown vectorially in figure 12a, we want to be able to select two phases, one from each differential amplifier. The selected phase from each differential amplifier will then be input to each side of an output stage differential amplifier. The way we select a particular phase for each differential amplifier is to use MESFETs as variable resistors and implement them as shown in figure 12b. Figure 13 shows the MESFETs characteristics and how the FET can be used as a gate voltage dependent resistor. For Vgs = 0 we have lower resistance than for Vgs = -1, as seen in figure 13.

The point between the two FETs in figure 12b can thus take on any value between the two outputs of the differential amplifier. The value will be determined by the gate potentials of the modulating FETs. Example signals between the modulating FETs are shown in figures 14 a and b

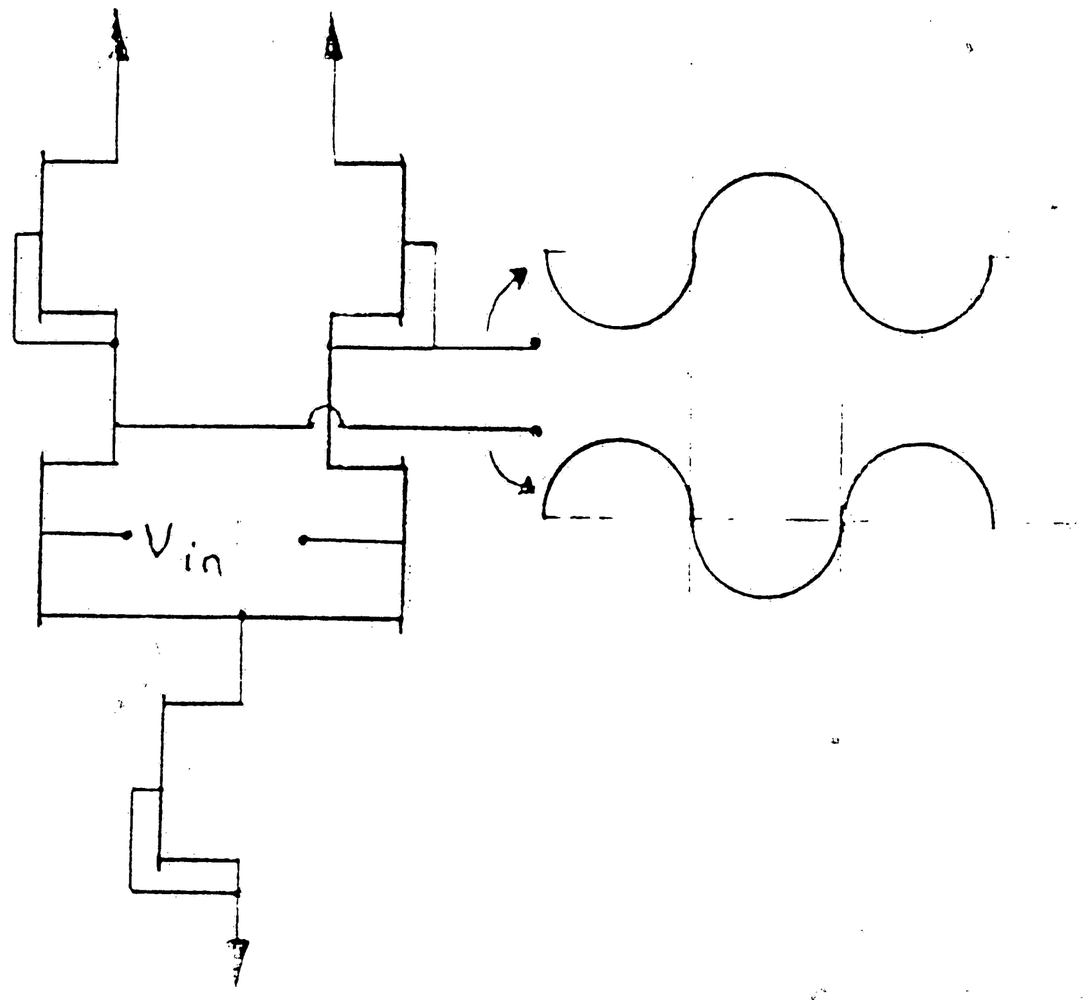


Fig. 8

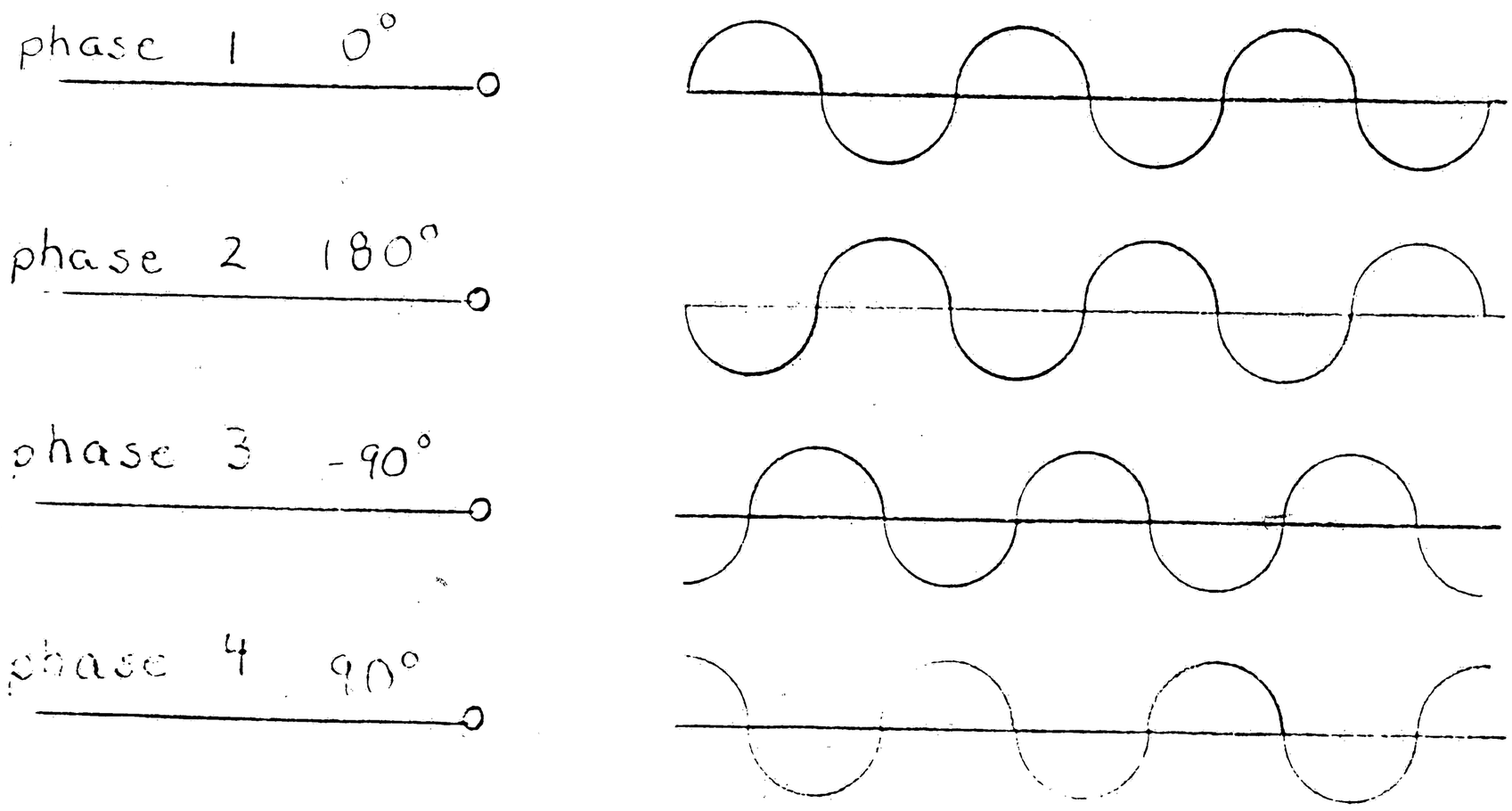


Fig. 9

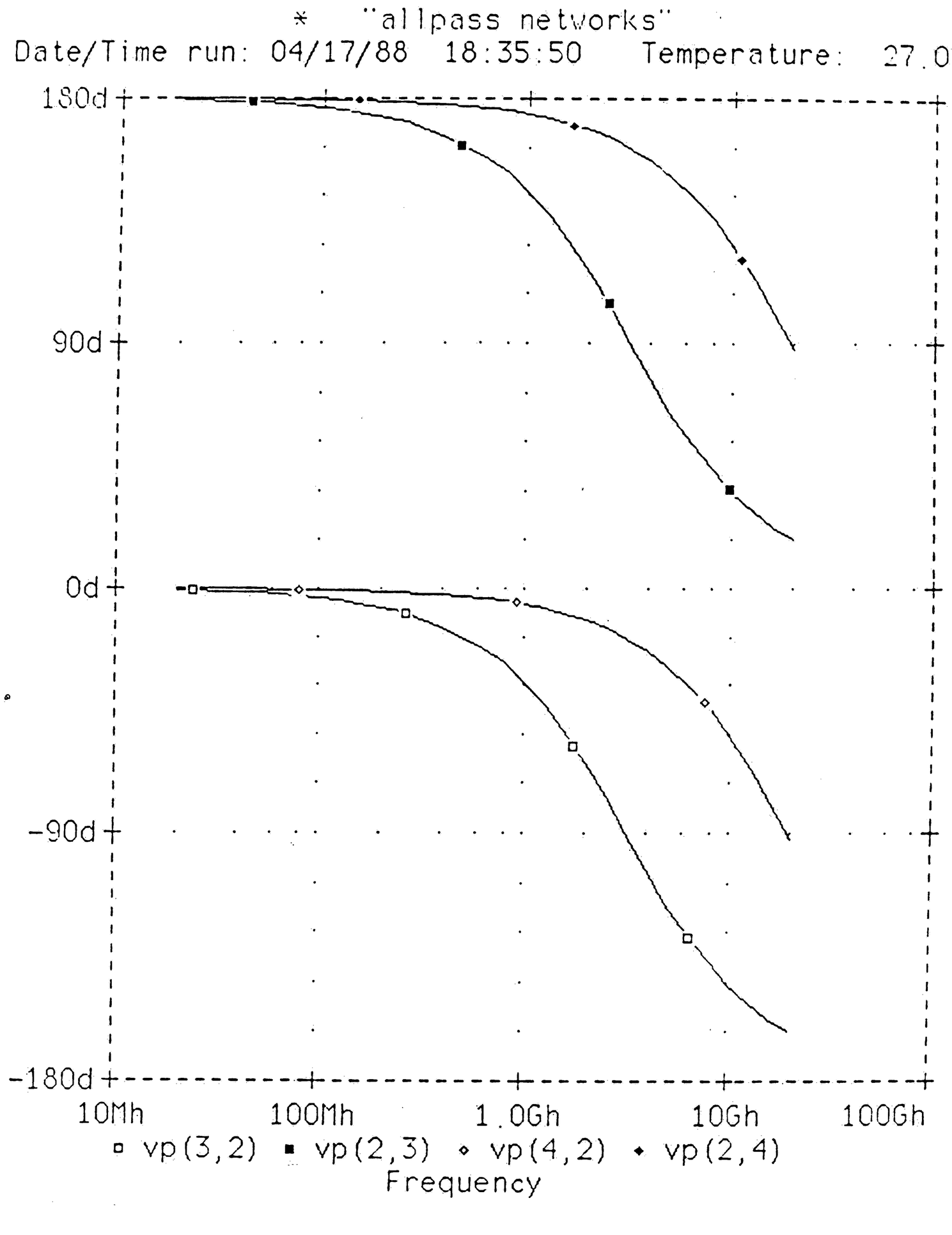

* "allpass networks"
Date/Time run: 04/17/88 18:35:50 Temperature: 27.0
180d
90d
0d
-90d
-180d
10Mh
100Mh
1.0Gh
10Gh
100Gh
▫ vp(3,2) ▪ vp(2,3) ◇ vp(4,2) ◆ vp(2,4)
Frequency

Fig. 10

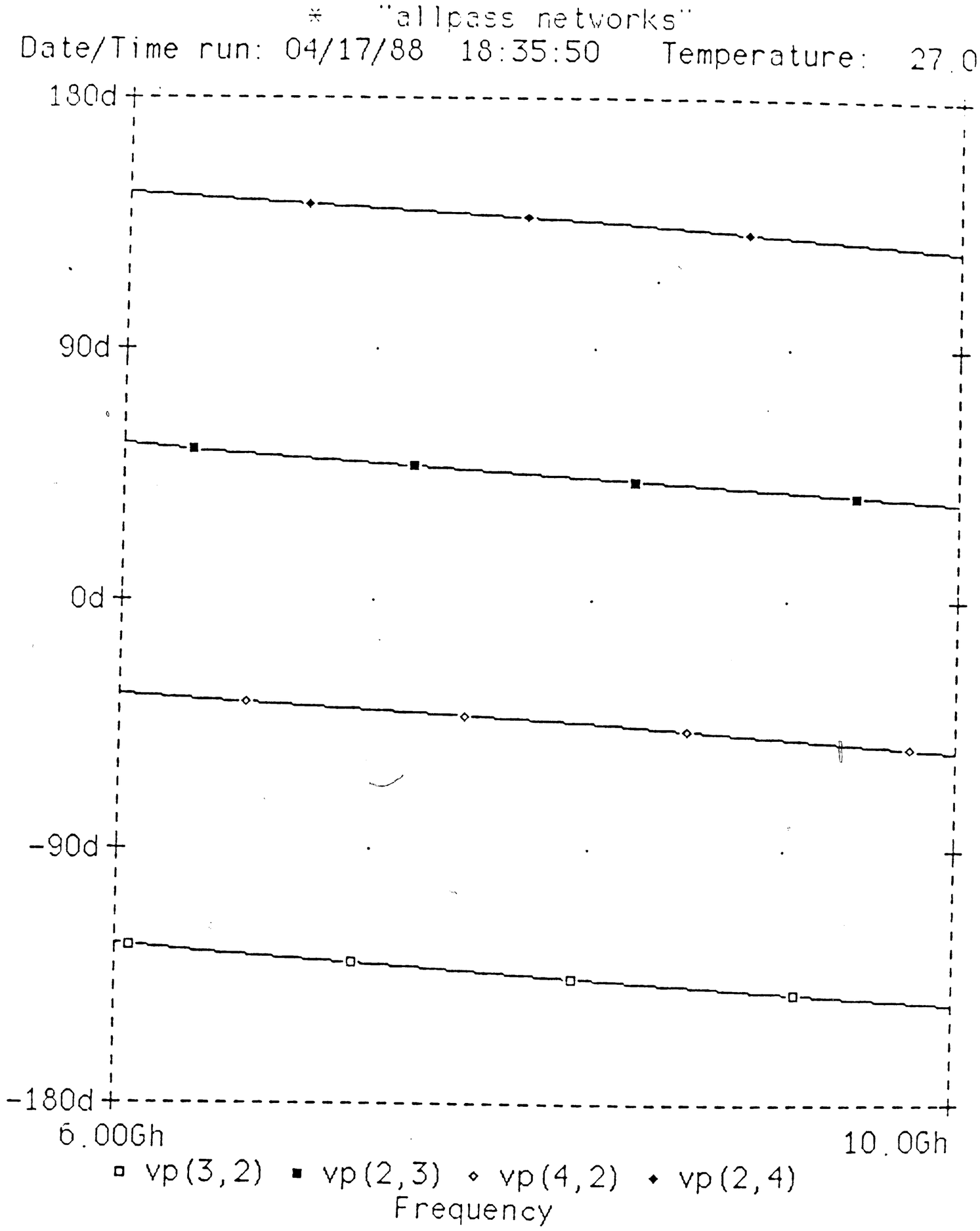

* "allpass networks"
Date/Time run: 04/17/88 18:35:50 Temperature: 27.0
180d
90d
0d
-90d
-180d
6.00Gh
10.0Gh
□ vp(3,2) ■ vp(2,3) ◇ vp(4,2) ◆ vp(2,4)
Frequency

Fig. 11

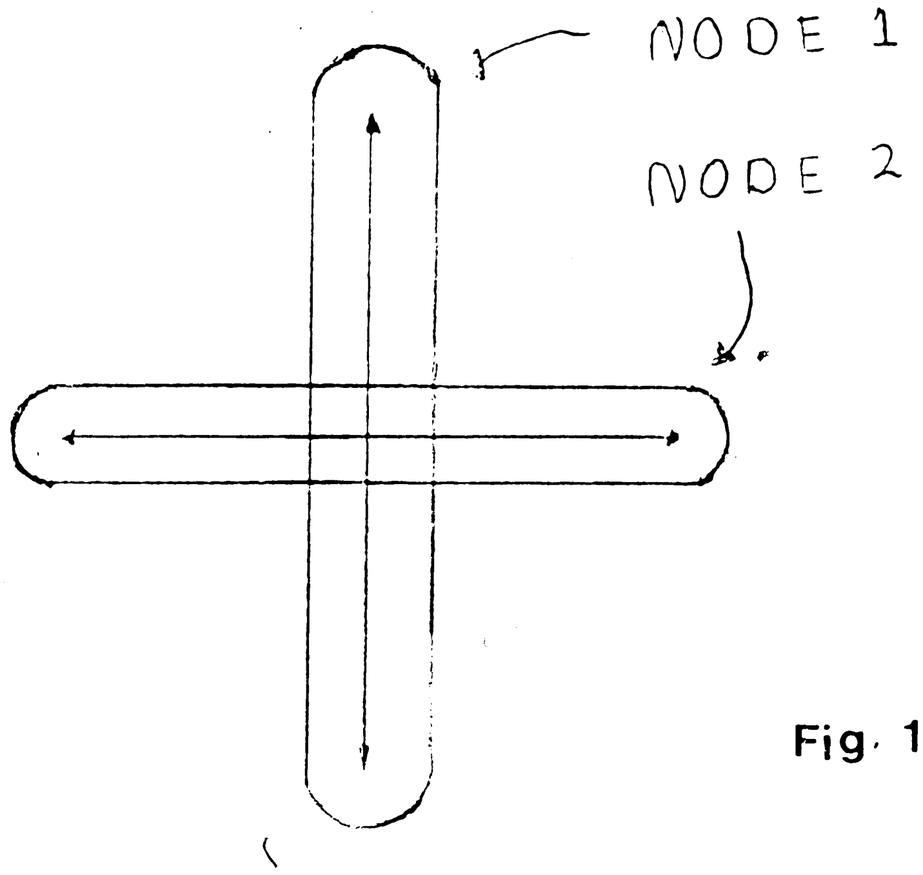
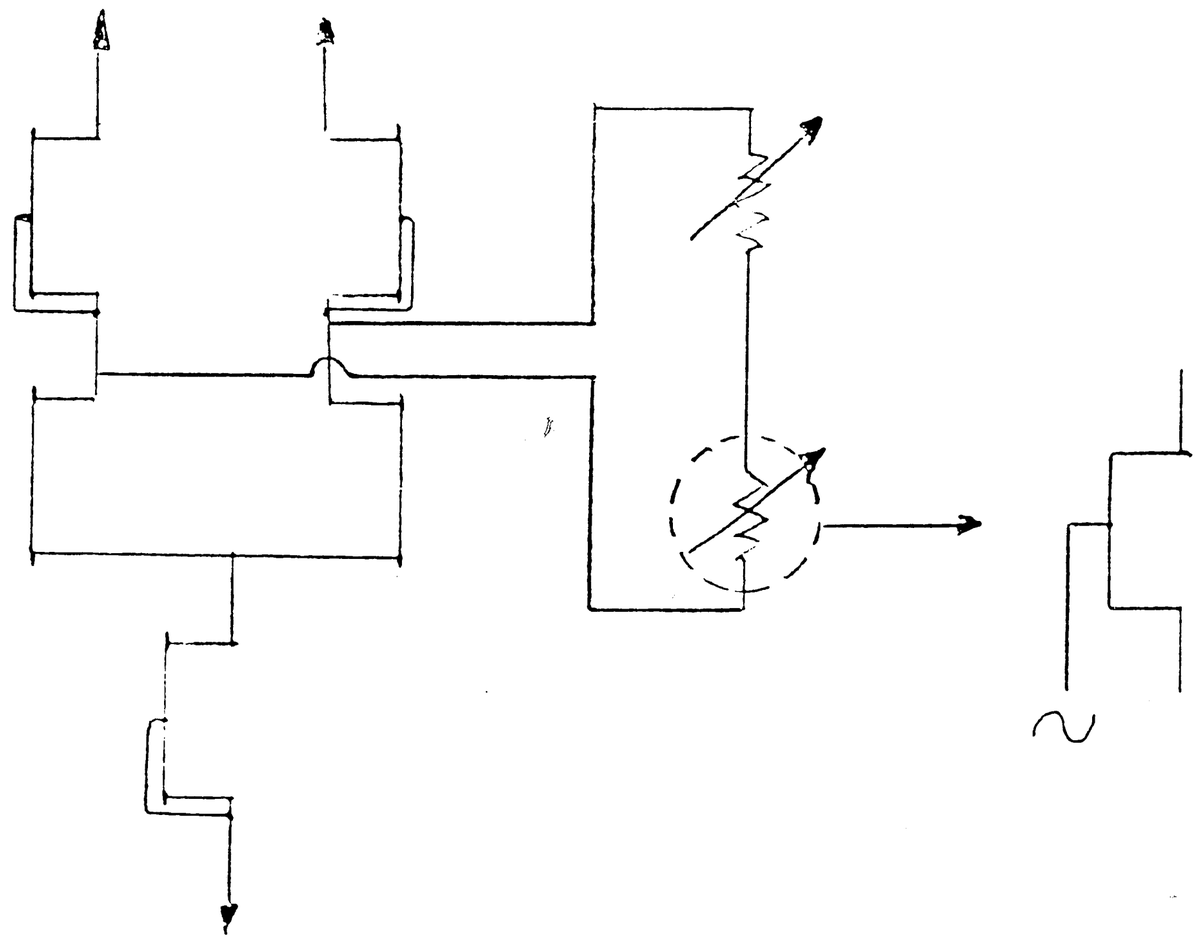


Fig. 12a

Fig. 12b



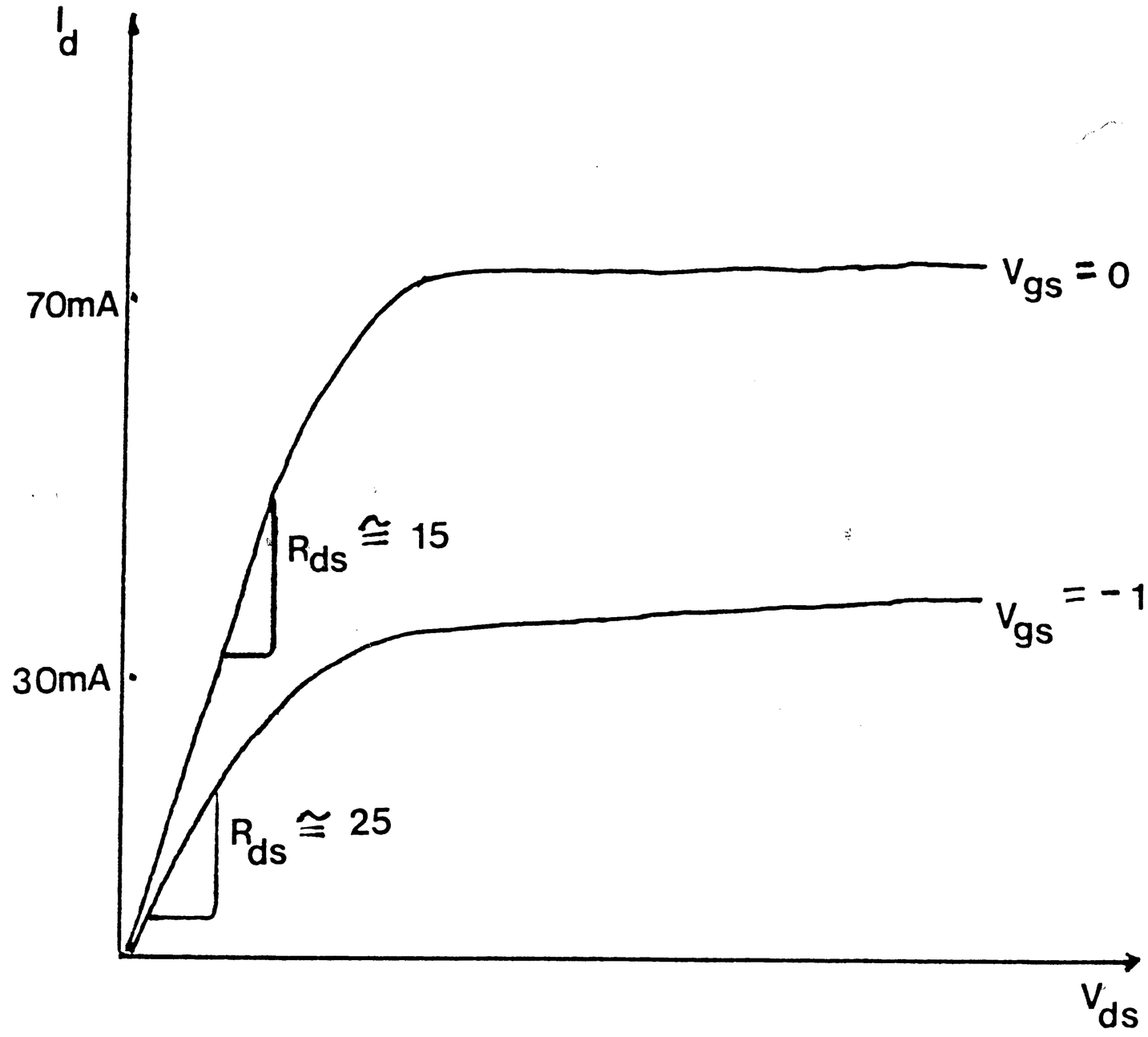


Fig. 13

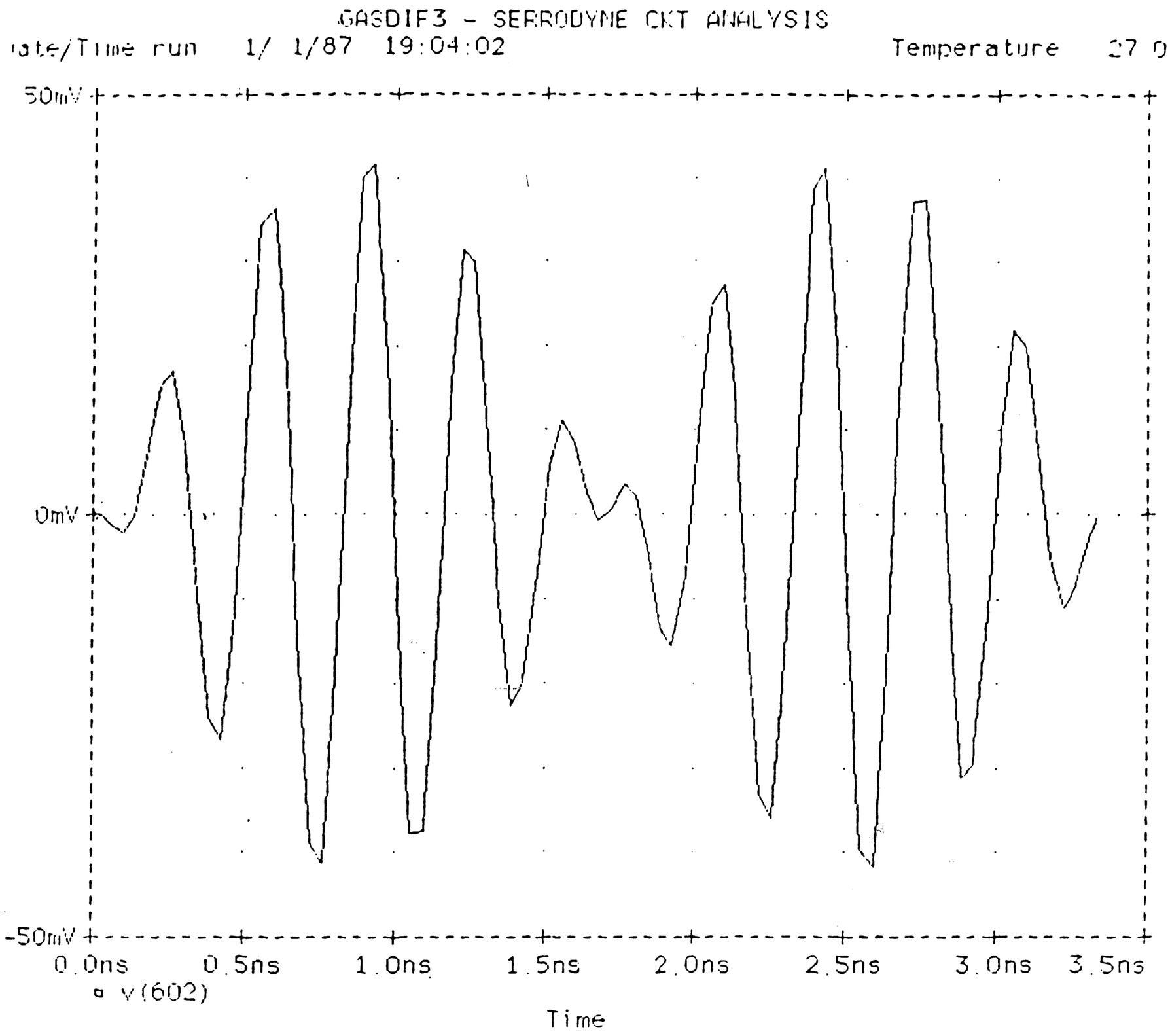

GASDIF3 - SERRODYNE CKT ANALYSIS
Date/Time run 1/ 1/87 19:04:02
Temperature 27.0
50mV
0mV
-50mV
0.0ns
0.5ns
1.0ns
1.5ns
2.0ns
2.5ns
3.0ns
3.5ns
V(602)
Time

Fig. 14a

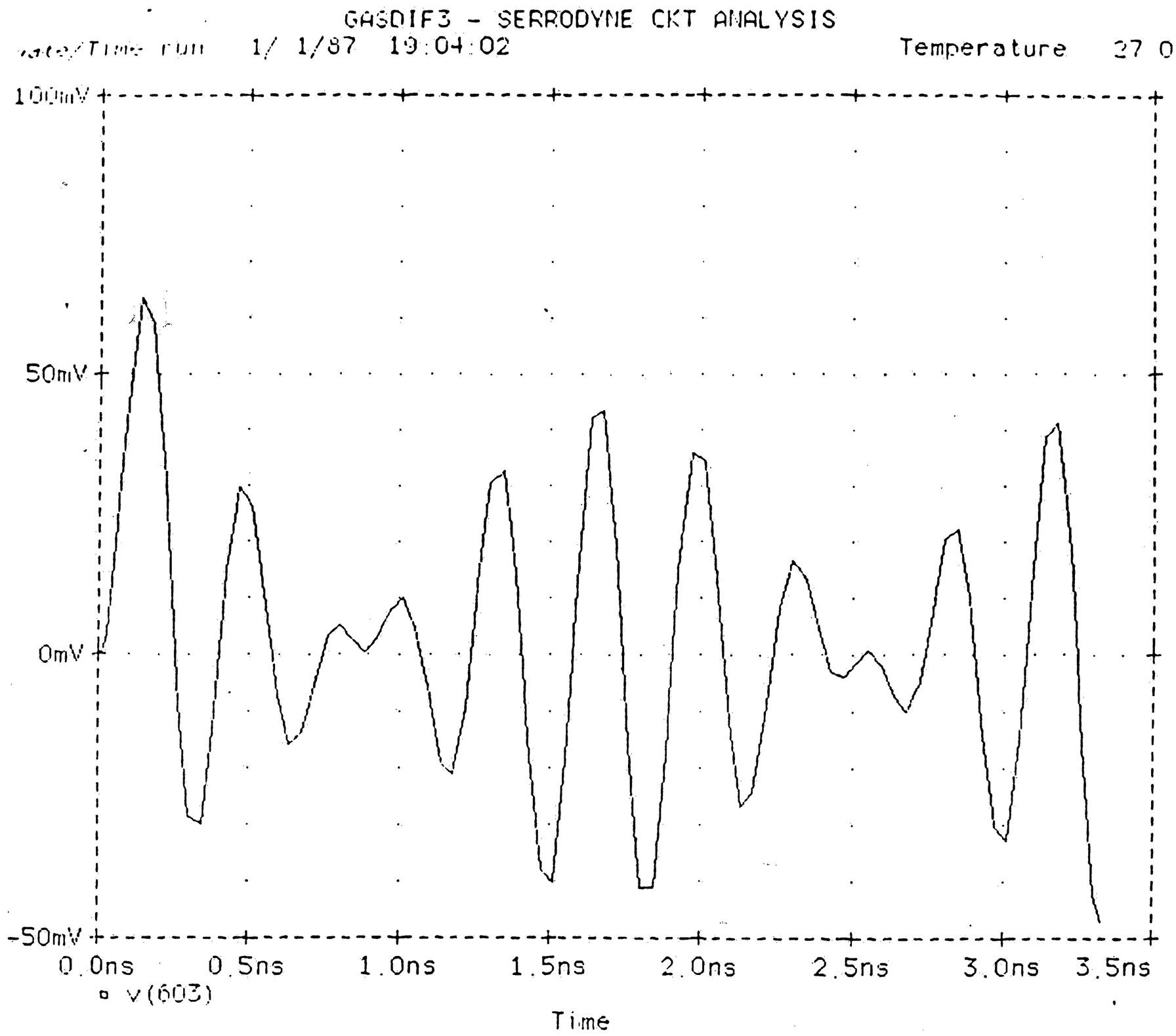

GASDIF3 - SERRODYNE CKT ANALYSIS
Date/Time run: 1/ 1/87 19:04:02
Temperature: 27.0
100mV
50mV
0mV
-50mV
0.0ns
0.5ns
1.0ns
1.5ns
2.0ns
2.5ns
3.0ns
3.5ns
V(603)
Time

Fig. 14b

for quadrature modulating signals. Figure 15 shows the two signals together. By comparing figures 14 a and b one can see that these signals are also in quadrature. This means that one is maximum while one is zero, thus the difference between the two is constant. Finally the signals obtained from each differential amplifier by the modulating FETs are input to an output stage differential amplifier. By changing the gate voltages on the MESFETs we can change their resistance and obtain an output phase between 0 and 360 degrees. In addition, if we apply sinusoidal quadrature signals to the gates of the modulating MESFETs we will be constantly changing the phase of the output signal. This constant change in phase will be seen as a frequency shift, so our serrodyne phase shifter can be used as a frequency modulator.

Performance

The outputs of the first differential amplifier are about three times larger than the gate inputs. The allpass networks pass a voltage magnitude of half the input magnitude. The modulators also contribute some loss. By driving the gates of the modulators with a large signal, without drawing gate current, we can limit the loss. The overall gain expected is between 0dB and 3dB.

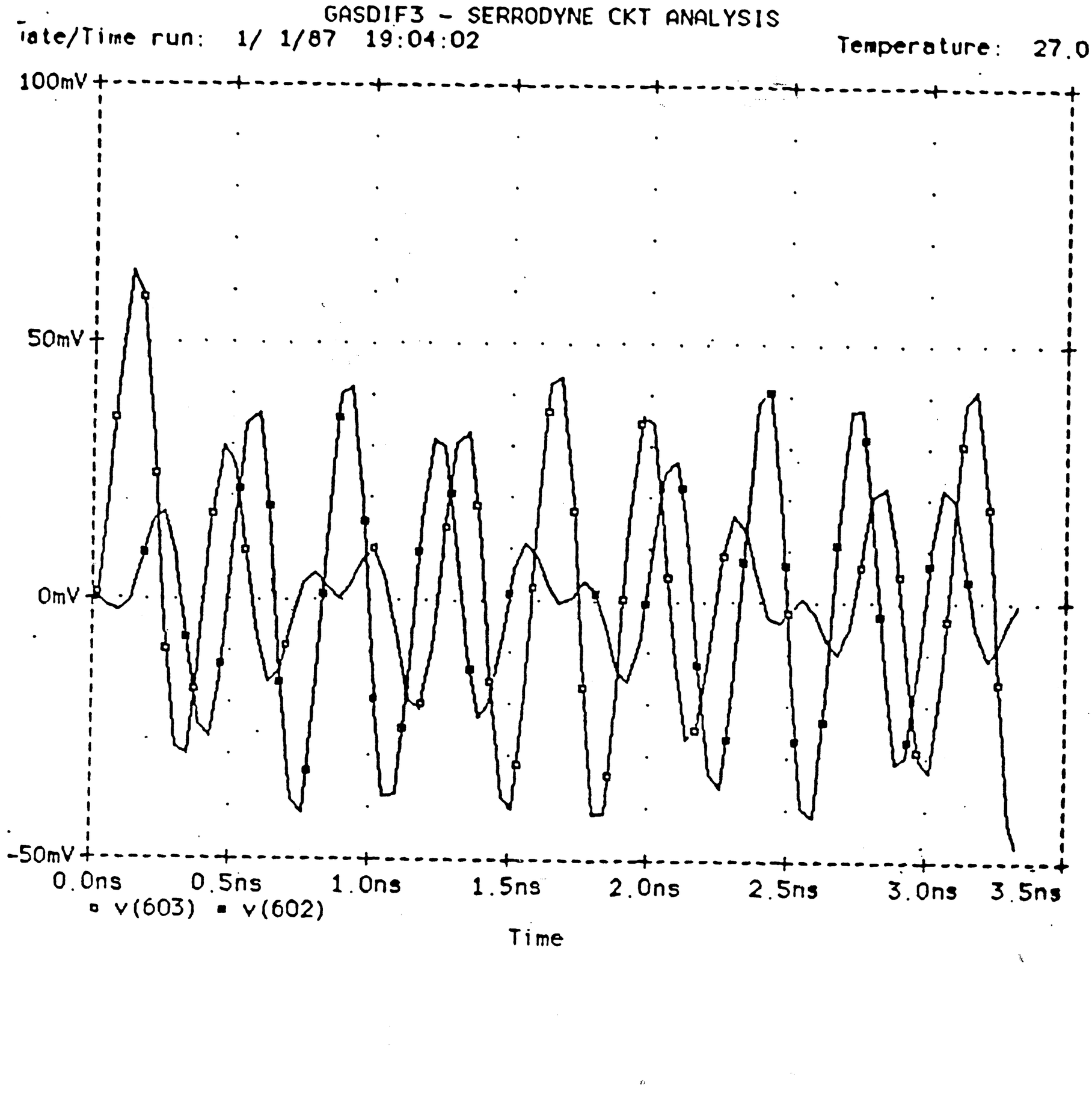

GASDIF3 - SERRODYNE CKT ANALYSIS
Date/Time run: 1/ 1/87 19:04:02
Temperature: 27.0
100mV
50mV
0mV
-50mV
0.0ns
0.5ns
1.0ns
1.5ns
2.0ns
2.5ns
3.0ns
3.5ns
v(603)
v(602)
Time

Fig. 15

LINEAR DOUBLE BALANCED MESFET MIXER

General Information

Classical mixers use the superposition of a radio frequency(R.F.) signal and a local oscilator(L.O.) on a diode to obtain an intermediate frequency(I.F.) signal. Since the diode has a nonlinear characteristic, the superposition of the L.O. and R.F. on the diode generates many harmonics of the sum and difference of the two signals. The signals of interest in mixers are for IF=LO−RF and IF=LO+RF. After the diode we require embedding impedances that filter out all the unwanted sideband frequencies.

Diodes are not the only devices used for mixing signals [6]. In fact, any nonlinear circuit element can be used as a mixer. This brings us to the topic of MESFET mixers where the nonlinear transconductance can be used to mix signals. There are two basic types [7], the gate mixer and the drain mixer. For the gate mixer there are again two types. There is a dual-gate mixer where the R.F. and L.O. are each applied to one of the FET gates. In this mixer the R.F. and L.O. are modulating the channel current at the same time to obtain the frequency conversion. In the single gate mixer the superposition of the R.F. and L.O. are applied to the gate and the nonlinear transconductance will

mix the two signals. In the drain mixer the L.O. is applied to the gate while the R.F. is applied to the drain. In this mixer the R.F. in the drain mixes with the channel current, which is modulated by the L.O. signal at the gate.

In all of the above circuits the I.F. is fibtered from the drain and we obtain gain by having a bias from drain to source. In general the MESFET mixers give lower intermodulation compared to diode mixers because the nonlinear transconductance of the MESFET is smaller compared to that of the nonlinear diode. Since the MESFET mixers are not as nonlinear in the proposed mode pf operation, it will be less difficult to filter out the unwanted sidebands to obtain the desired intermediate frequency signal.

Operation of a Linear Double Balanced Mesfet Mixer

The linear double balanced GaAs MESFET MMIC mixer is shown in figure 16. This MESFET configuation is similar to the double balanced diode mixer. As stated before the most common way to obtain frequency conversion is to use a nonlinear element, however frequency conversion can be done by using an ideal switch. The MESFET structure in figure 16 uses the L.O. to switch on and off particular MESFET to obtain the frequency conversion. For one polarity of L.O. the R.F. will take one path and for the other polarity the

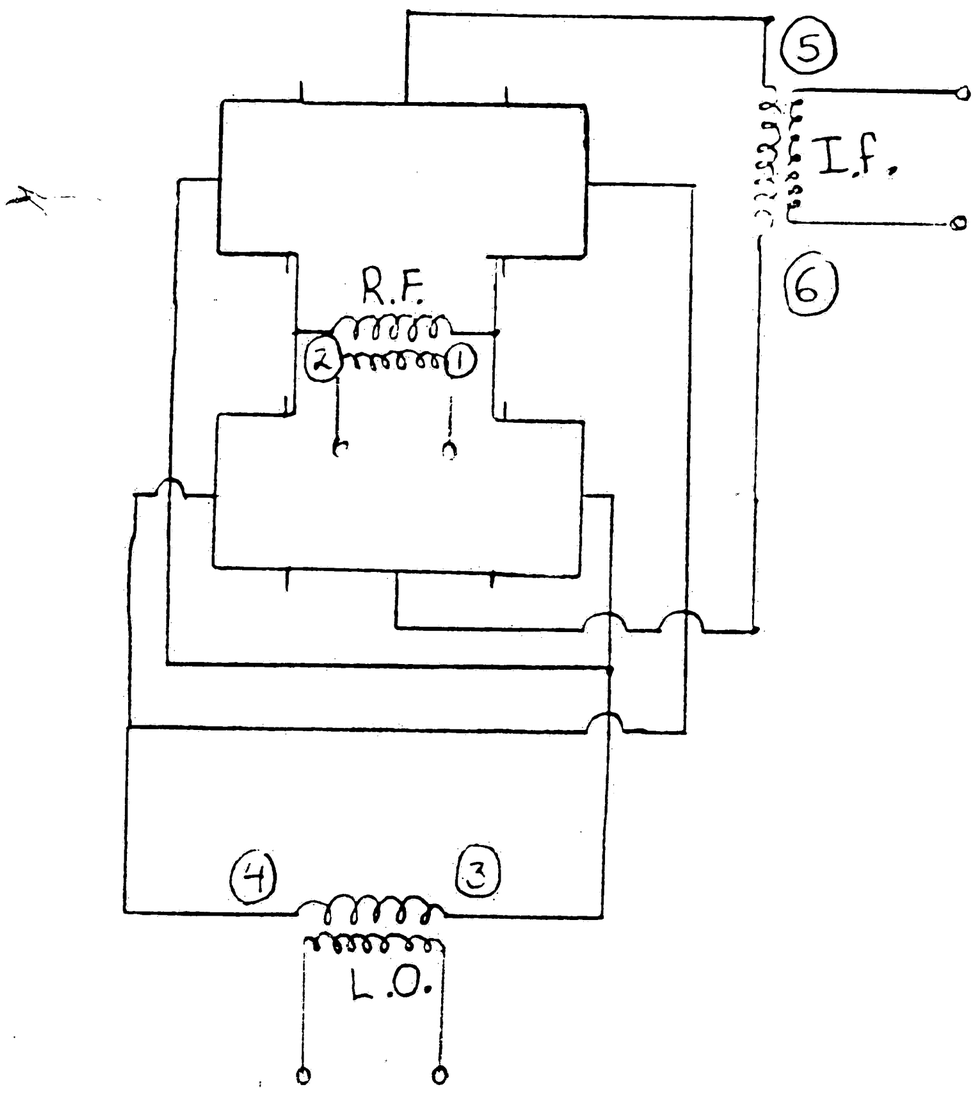


Fig 16

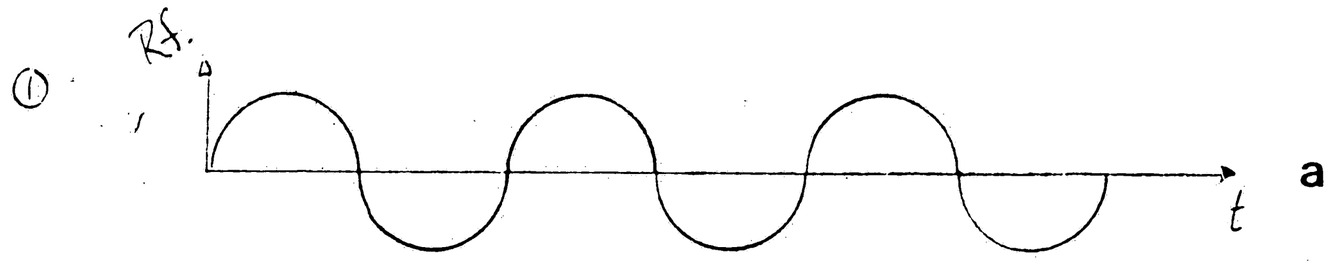
TBL. 1

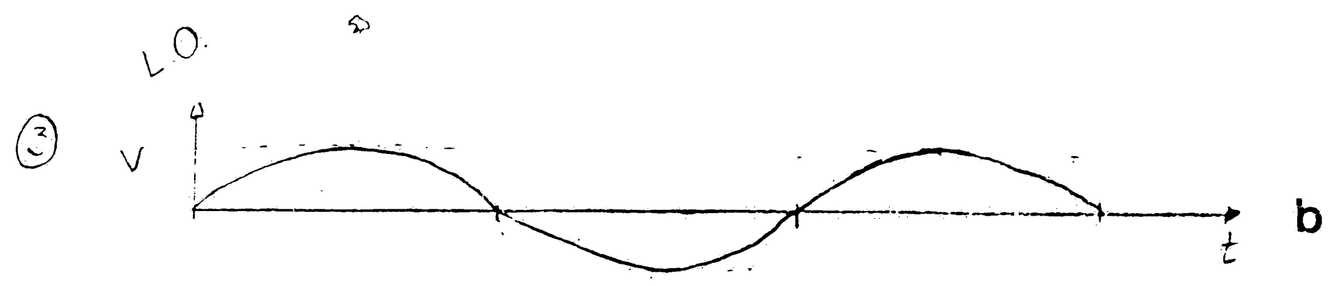
1	2	3	4	5	6
+	−	+	−	−	+
−	+	+	−	+	−
+	−	−	+	+	−
−	+	−	+	−	+

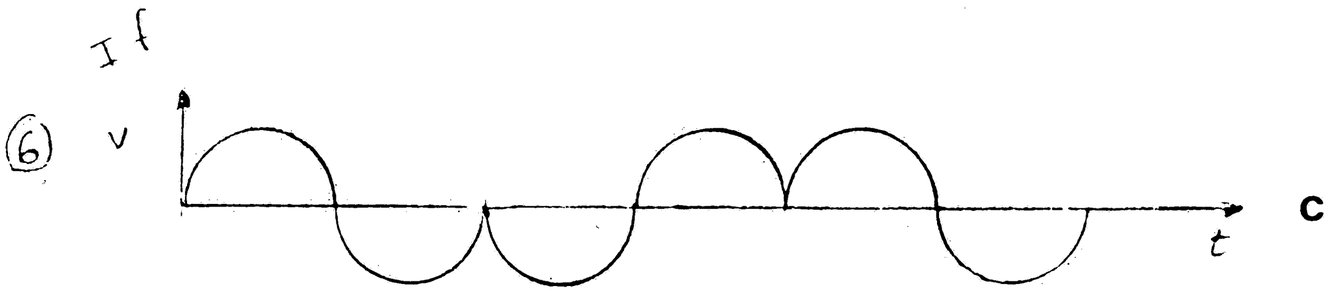
R.F. will take the other path. To see how we can obtain frequency conversion from this structure in figure 16 let us assume the polarities given in table 1. These polarities will give the signals in figure 17 a, b, and c.

What happens is that the local oscillator switches the direction of the R.F. signal. As shown in figure 17c, the I.F. may follow the R.F. for one polarity of L.O. but when the L.O. switches polarity the I.F. signal is 180 degrees out of phase with respect to the R.F. signal. The result shown in figure 17c shows the result of the MESFET mixer for the R.F. signal and L.O. signals given in figures 17a and 17b, respectively.

We can see that the I.F. contains both the sum and difference of the R.F. and local oscillator. A simulated result of the mixer is shown in figure 18. In this figure we have a 2GHz L.O. and a 3GHz R.F. signal. The I.F. signal clearly shows the sum and difference of the R.F. and L.O. signals. We can see the low frequency 1GHz difference signal with the higher 5GHz frequency sum signal riding on top of the low frequency signal. Since the mixer is double balanced we expect to have small spectral components at either the R.F. or L.O. frequencies. The fourier analysis is shown in figure 19 a and b, for the fundamentals of 1GHz and 5GHz respectively. As can be seen in 19 a and b, the largest spectral components are found at 1GHz, the







Figs. 17a, 17b, and 17c

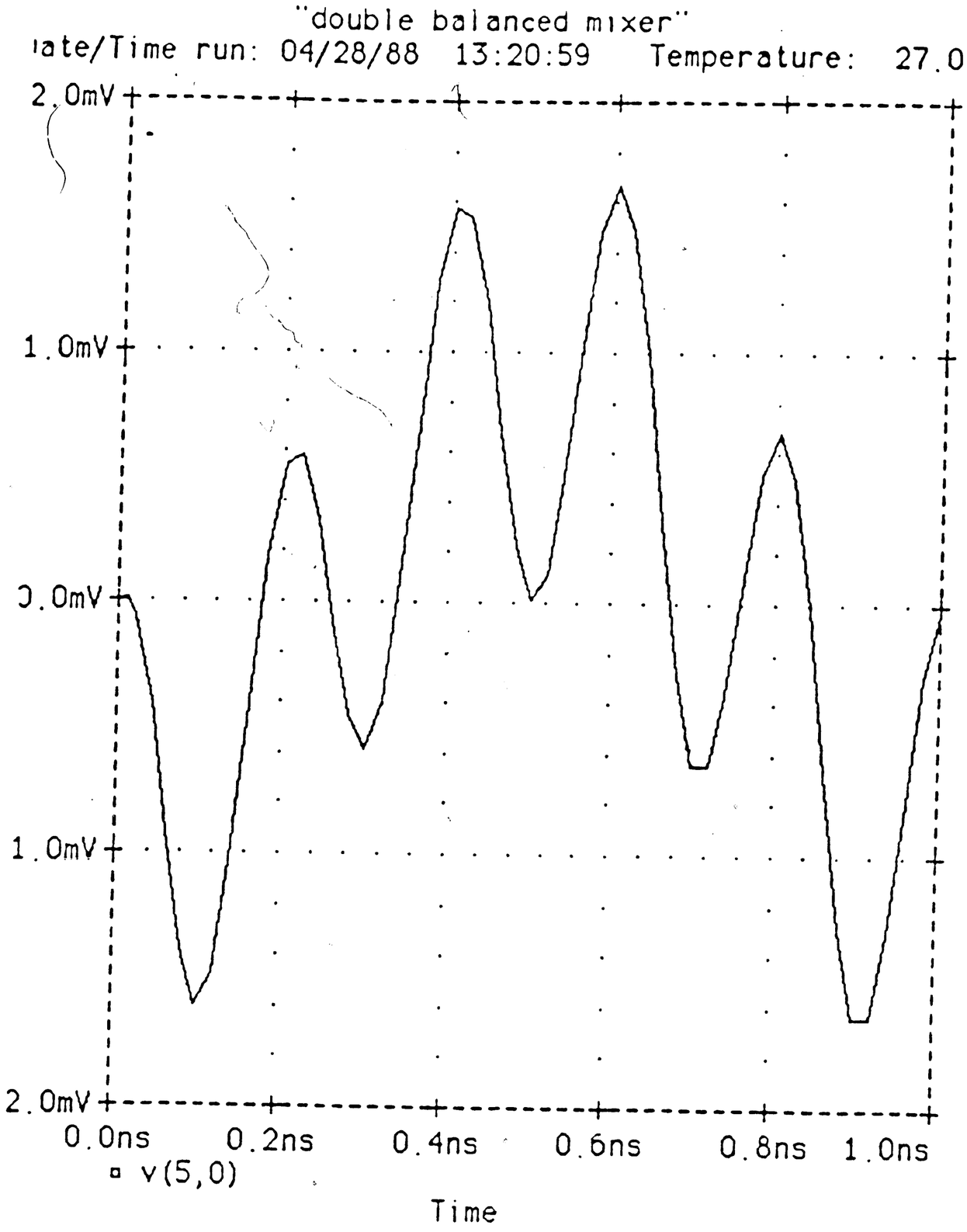

"double balanced mixer"
Date/Time run: 04/28/88 13:20:59 Temperature: 27.0
2.0mV
1.0mV
0.0mV
1.0mV
2.0mV
0.0ns
0.2ns
0.4ns
0.6ns
0.8ns
1.0ns
v(5,0)
Time

Fig. 18

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(5,0)

DC COMPONENT = 2.825812E-06

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000E+09	9.035E-04	1.000E+00	-9.406E+01	0.000E+00
2	2.000E+09	2.175E-05	2.407E-02	-1.023E+02	-8.287E+00
3	3.000E+09	2.254E-05	2.495E-02	-1.100E+02	-1.593E+01
4	4.000E+09	5.973E-05	6.611E-02	-5.568E+01	3.839E+01
5	5.000E+09	7.874E-04	8.715E-01	6.564E+01	1.597E+02
6	6.000E+09	3.819E-05	4.227E-02	6.095E+01	1.550E+02
7	7.000E+09	1.792E-05	1.984E-02	5.966E+01	1.537E+02
8	8.000E+09	1.220E-05	1.350E-02	5.895E+01	1.530E+02
9	9.000E+09	7.857E-06	8.696E-03	6.193E+01	1.560E+02

TOTAL HARMONIC DISTORTION = 8.760685E+01 PERCENT

a

LIST 134 04-27-88 19:30 ♦ MIXER.OUT
FOURIER COMPONENTS OF TRANSIENT RESPONSE V(5,0)

DC COMPONENT = -7.050254E-04

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	5.000E+09	8.970E-04	1.000E+00	8.437E+01	0.000E+00
2	1.000E+10	8.348E-05	9.306E-02	1.715E+02	8.710E+01
3	1.500E+10	5.468E-05	6.096E-02	1.772E+02	9.284E+01
4	2.000E+10	4.076E-05	4.544E-02	-1.792E+02	-2.636E+02
5	2.500E+10	3.250E-05	3.623E-02	-1.766E+02	-2.609E+02
6	3.000E+10	2.699E-05	3.009E-02	-1.743E+02	-2.586E+02
7	3.500E+10	2.309E-05	2.574E-02	-1.721E+02	-2.565E+02
8	4.000E+10	2.017E-05	2.249E-02	-1.701E+02	-2.544E+02
9	4.500E+10	1.791E-05	1.997E-02	-1.680E+02	-2.524E+02

TOTAL HARMONIC DISTORTION = 1.350080E+01 PERCENT

b

Figs. 19a and 19b

difference of the two frequencies, and 5GHz, the sum of the two frequencies.

Performance

The linear double balanced mixer will have some loss, because it is not a biased circuit. There is no bias because we want to stay in the linear region of the FET so we will have as little intermodulation as possible. In order to minimize the loss the L.O. should be as large as possible without forward biasing the gate-source of the FET, so there will be only a small channel resistance for the on FETs and a large resistance for the off FETs. This means the I.F. signal will be maximized.

FOUNDRY AND DESIGN RULES

General Information

When making a MMIC circuit one uses a technology which is defined by the foundry doing the fabrication. For a specific technology there is a given set of mask levels, each with its own purpose. The different mask levels can include a shallow N implant, deep N+ implant, ohmic metal, gate metal, 1st metal plating, capacitor dielectric, dielectric via, air bridge via, 2nd metal plating, backside via and backside metal. Each technology has a set of design rules which describes the minimum distances between each mask level. The mask levels used in this thesis are shown in figure 20.

Resources at Lehigh and Technology File

The MMICs designed for this thesis were done with a technology file and design rule book from Harris Microwave Semiconductor. The GDS2 technology file was read into the Valid system of the VLSI laboratory. LED of the Valid system, which stands for layout editor, was used for the layout.

The technology file contained the different mask levels and a library of devices which include transistors, capacitors, resistors, inductors, diodes, and transmission

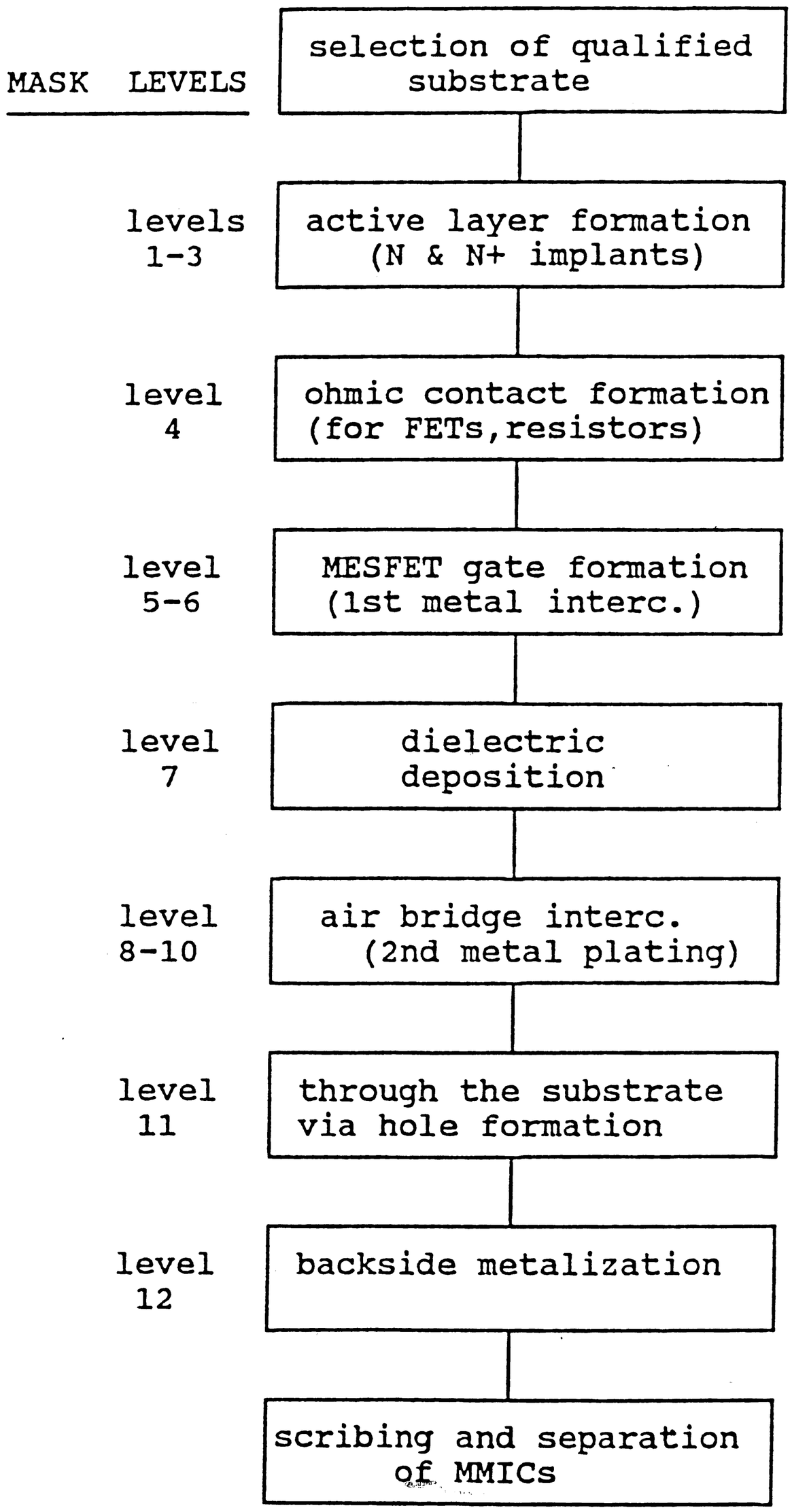

MASK LEVELS
selection of qualified substrate
levels 1-3
active layer formation (N & N+ implants)
level 4
ohmic contact formation (for FETs,resistors)
level 5-6
MESFET gate formation (1st metal interc.)
level 7
dielectric deposition
level 8-10
air bridge interc. (2nd metal plating)
level 11
through the substrate via hole formation
level 12
backside metalization
scribing and separation of MMICs

Fig. 20

lines. In general the resistors, capacitors and transmission lines are easily made using the design rules; however, the transistors and spiral inductors in the library will be used in the layout instead of making new designs. The reason for this is the design rule book contains S parameter data on these devices which can be used to derive an equivalent circuit. If we were to build, for example, our own FET we would have to rely on a theoretical model with no measured data to compare with for accuracy. Examples FETs and spiral inductors from the technology file are shown in figures 21 and 22, respectively. Figures 23 and 24 show examples of resistors and capacitors made for the layouts in this thesis.

Simulating FET Characteristics

In order to simulate the circuits it was necessary to extract parameters from the layout and the design rule book. When simulating, for example, the differential amplifiers, the I-V characteristics in the design rule book were matched to a FET model in SPICE. The design rule FET characteristics are shown in figure 25 and the SPICE characteristics are shown in figure 26. With the correct MESFET model in SPICE we can be sure that we have accurate performance predictions. Also the SPICE FET characteristics can be used for the AC, DC and transient analysis of the

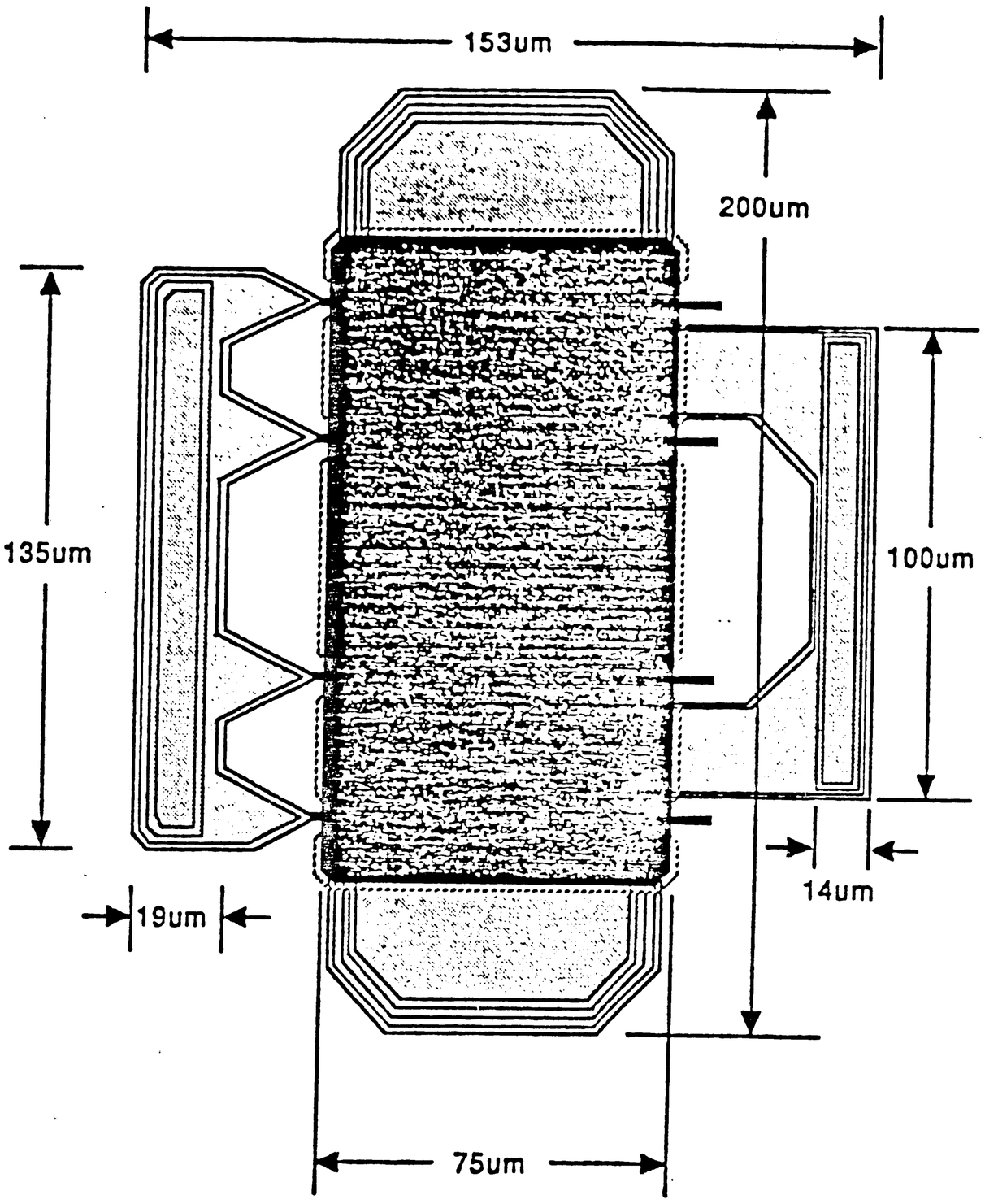


Fig. 21

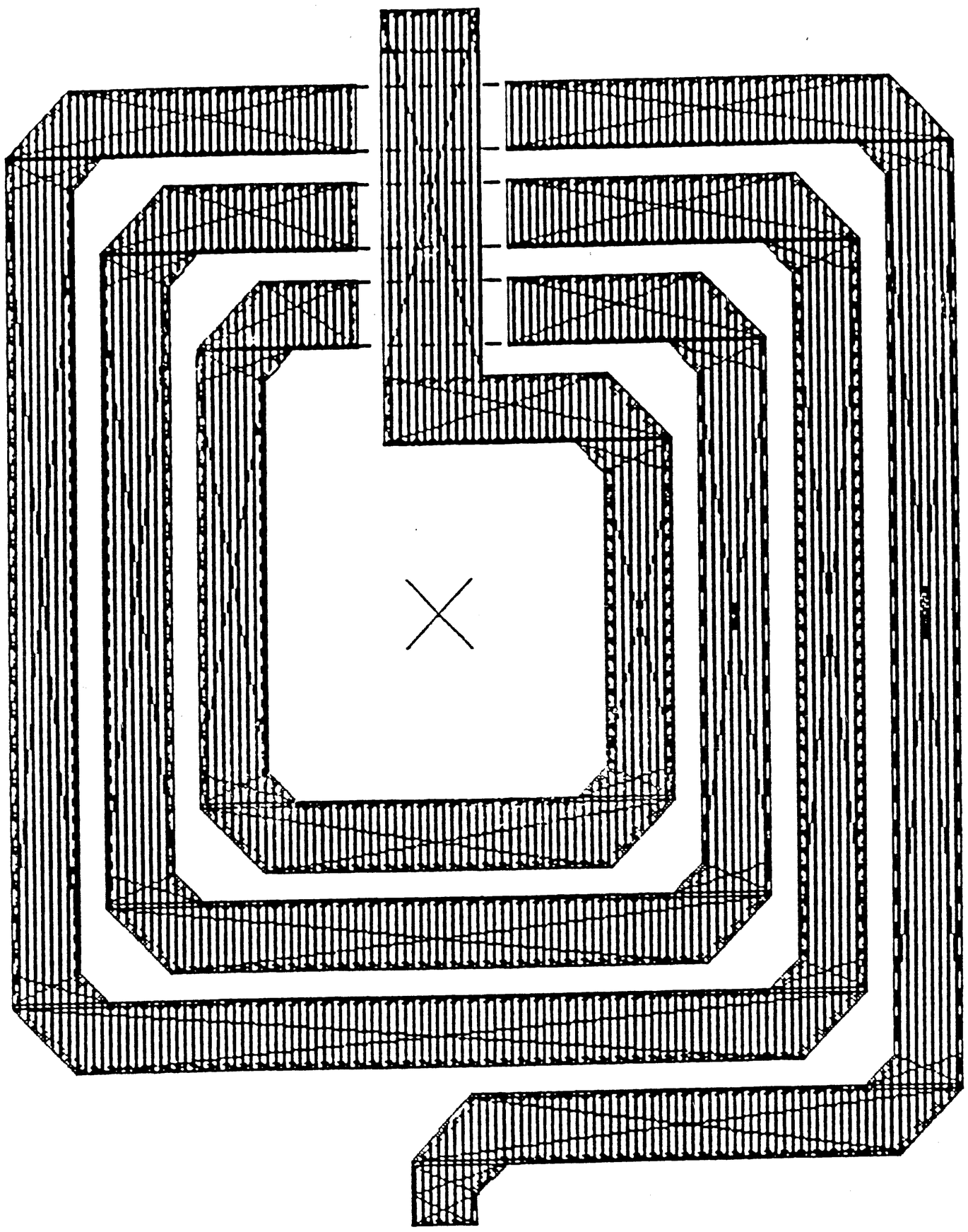


Fig. 22

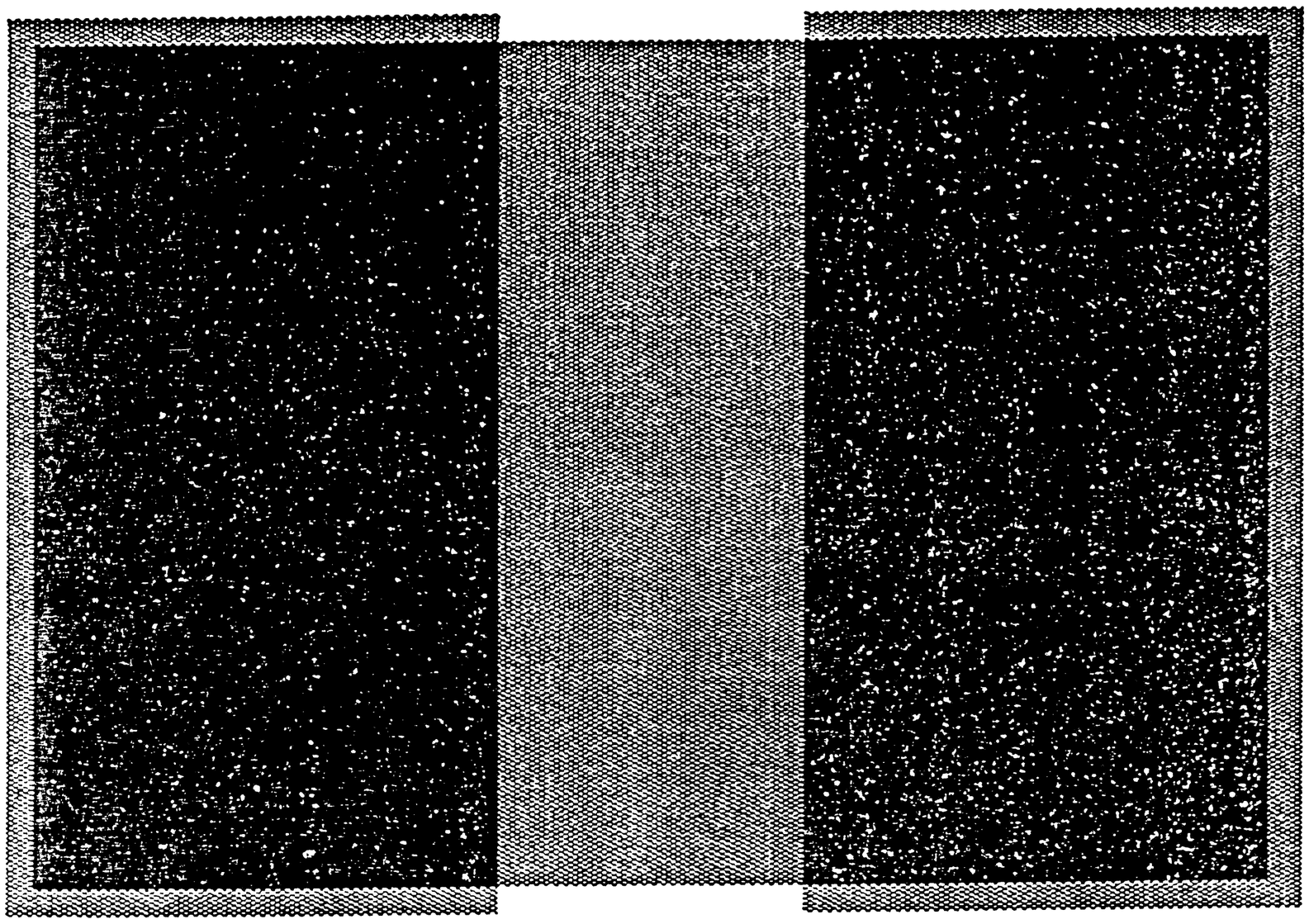


Fig. 23

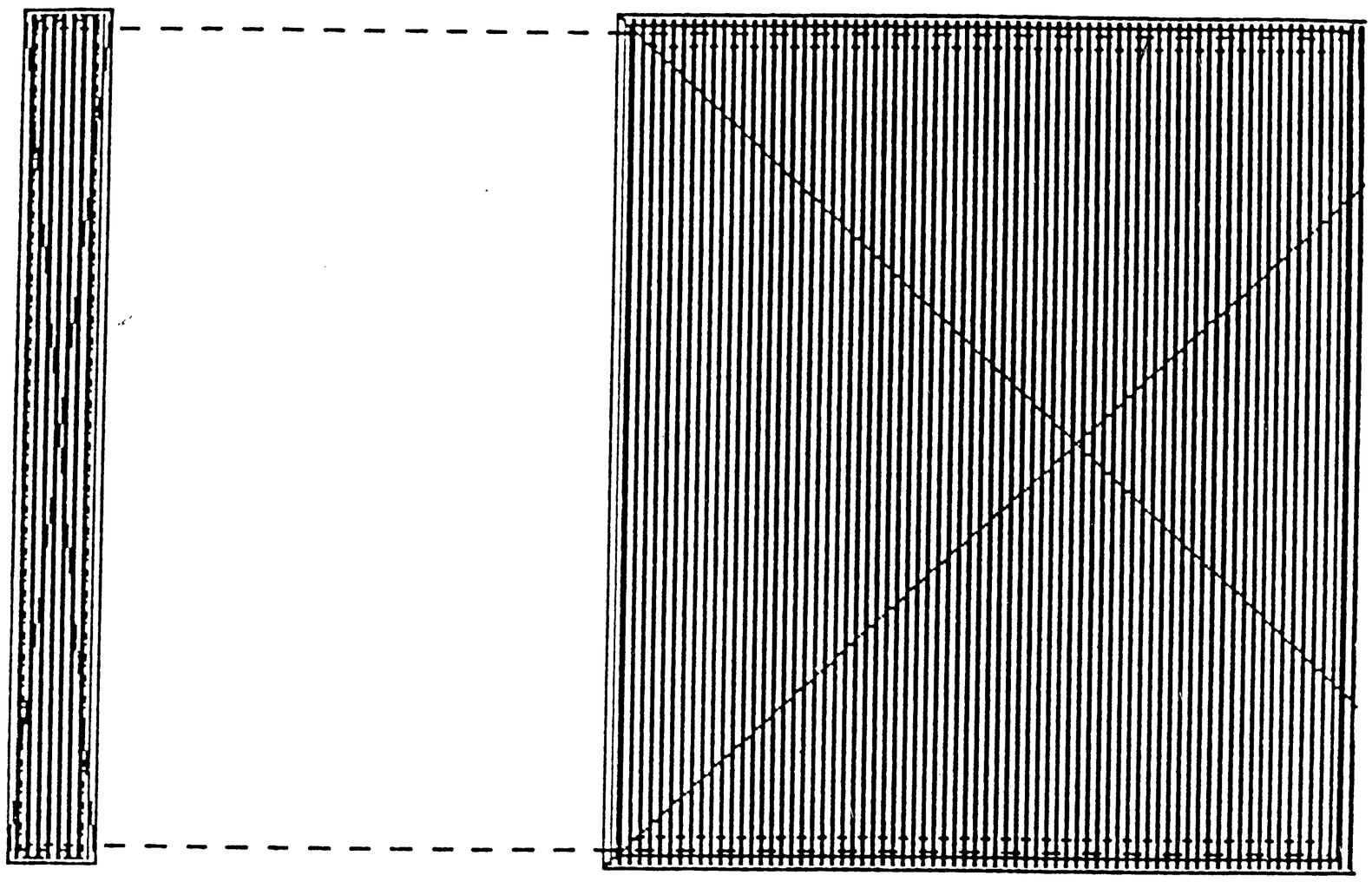


Fig. 24

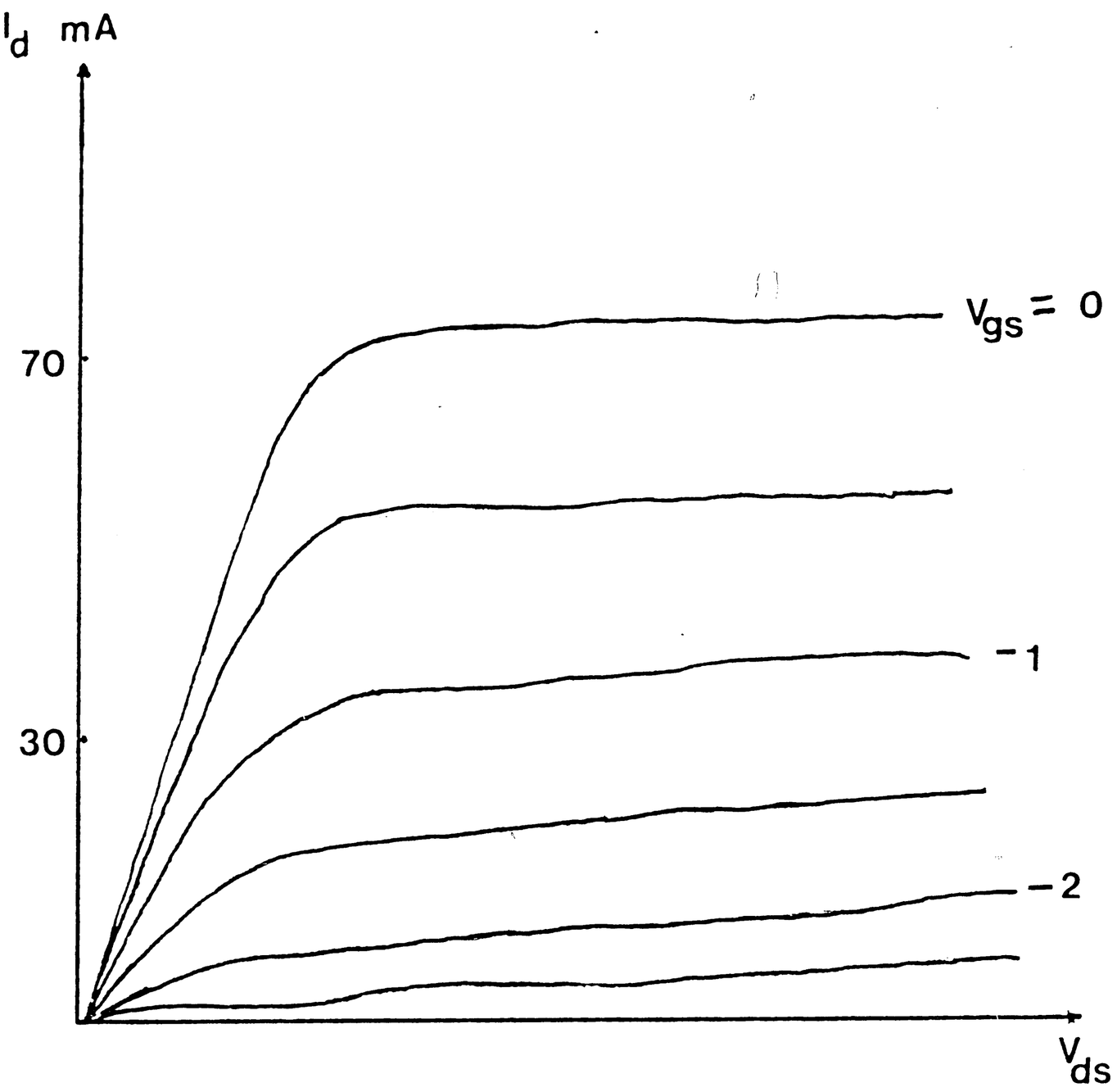


Fig. 25

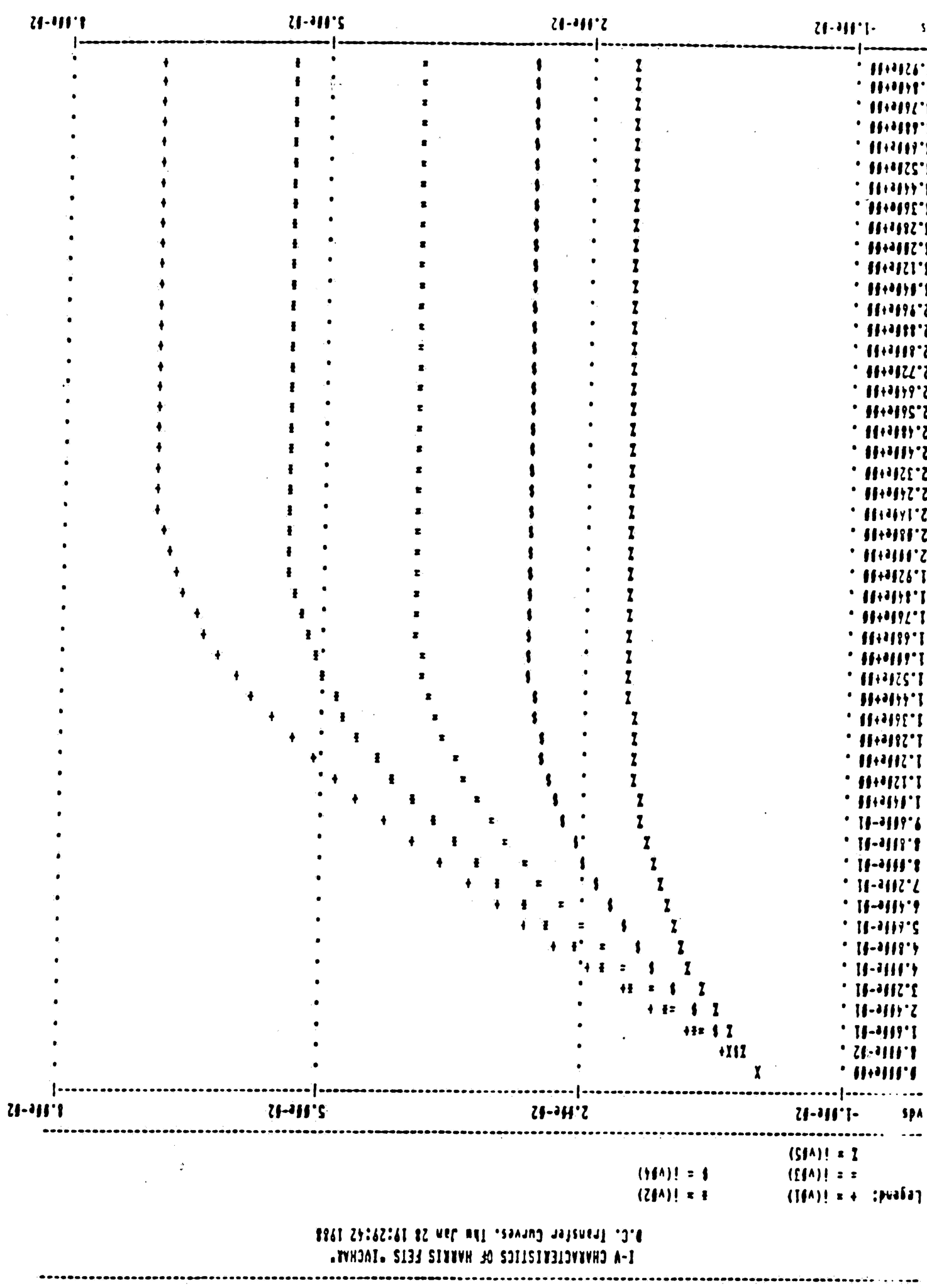

I-V CHARACTERISTICS OF HARRIS FETS "IVCHAR"
B.C. Transfer Curves. Tue Jan 28 19:29:42 1988
Legend: + = i(V81) # = i(V82)
= = i(V83) $ = i(V84)
Z = i(V85)
Vds -1.00E-02 2.00E-02 5.00E-02 8.00E-02
9.000E+00
8.000E-02
1.600E-01
2.400E-01
3.200E-01
4.000E-01
4.800E-01
5.600E-01
6.400E-01
7.200E-01
8.000E-01
8.800E-01
9.600E-01
1.040E+00
1.120E+00
1.200E+00
1.280E+00
1.360E+00
1.440E+00
1.520E+00
1.600E+00
1.680E+00
1.760E+00
1.840E+00
1.920E+00
2.000E+00
2.080E+00
2.160E+00
2.240E+00
2.320E+00
2.400E+00
2.480E+00
2.560E+00
2.640E+00
2.720E+00
2.800E+00
2.880E+00
2.960E+00
3.040E+00
3.120E+00
3.200E+00
3.280E+00
3.360E+00
3.440E+00
3.520E+00
3.600E+00
3.680E+00
3.760E+00
3.840E+00
3.920E+00

Fig. 26

circuits. The S parameter information in the design rule book can be used in programs like Super Compact for gain and stability information.

R and C Values

The values of R and C for the allpass networks were determined from the design constants in the design rule book. Appendix C shows some of these design constants and Appendix D shows how these design constants were used to determine the dimensions to be used in the layout. The lengths/side for the 1pf and .165pf capacitors were 59.5um and 24.5um, respectively. For a length of 11.25um and a width of 30um the resistance for an N+ resistor is 50.167 ohms.

LAYOUT FOR MMIC MIXER AND PHASE SHIFTER

Serrodyne Phase Shifter Layout

The layout for the serrodyne phase shifter will now be discussed. Figure 27 shows the block diagram form of the serrodyne phase shifter. This block diagram form is similar to figure 3. The difference is that figure 27 has a second allpass network that will establish four quadrature modulators. As stated in the operation section we need the quadrature modulating signals if we want to get a frequency shift. Figure 27 shows the input signal coming from the left and the modulating signal coming from the right. When this is implemented with FETs it looks as shown in figure 28. The final layout of this circuit is shown in figure 29.

There are some nice features about the serrodyne layout. As can be seen in figure 29 the layout of the phase shifter is very symmetrical. When designing MMICs you must be careful about transmission line lengths because different lengths can cause undesirable phase delays. As can be seen in the layout the line lengths are very symmetric, thus we should have no problems with parasitics on the different lines causing undesirable effects. The reason for this is, as stated before, the symmetry of the layout.

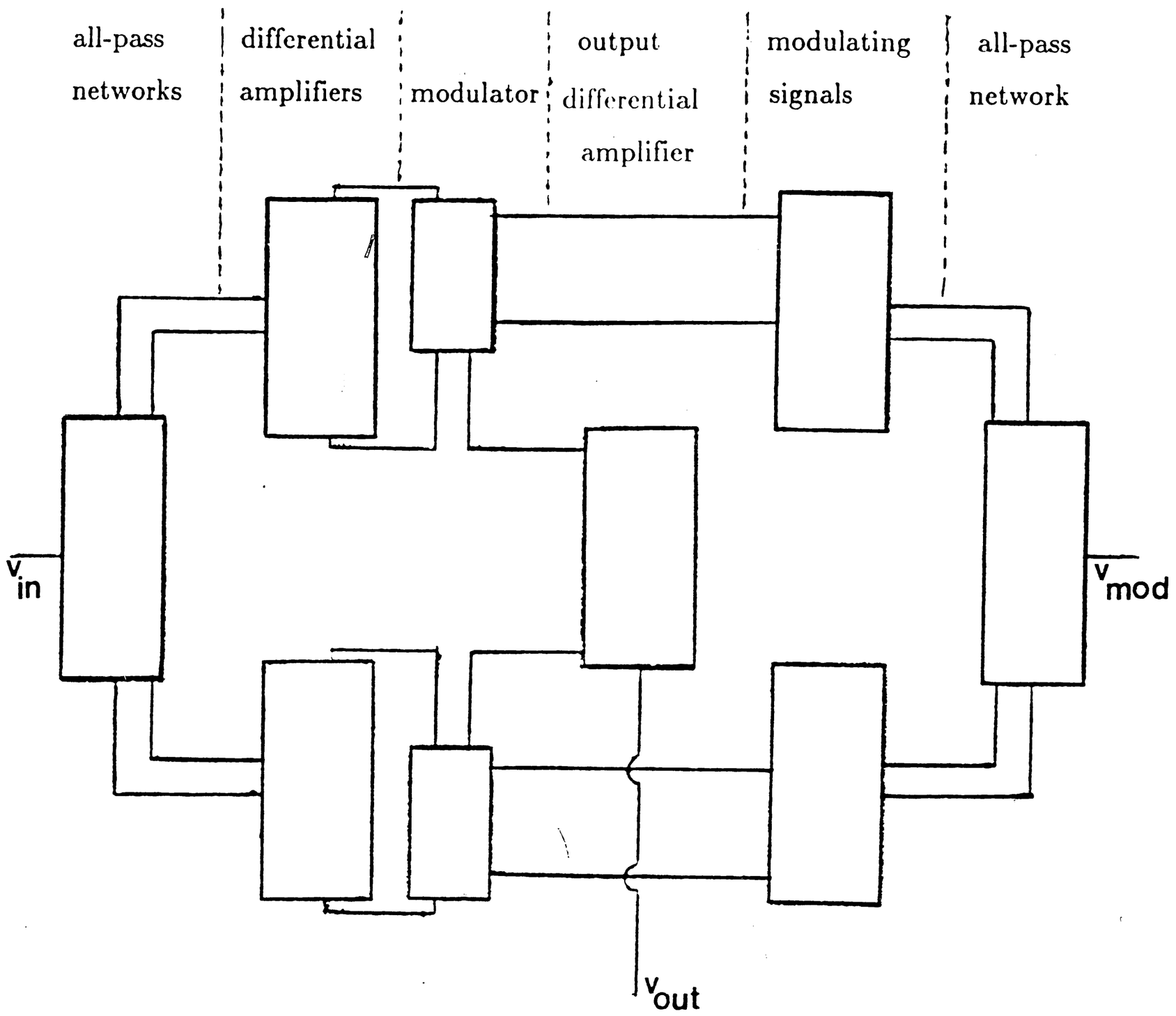

all-pass networks
differential amplifiers
modulator
output differential amplifier
modulating signals
all-pass network
v_{in}
v_{mod}
v_{out}

Fig. 27

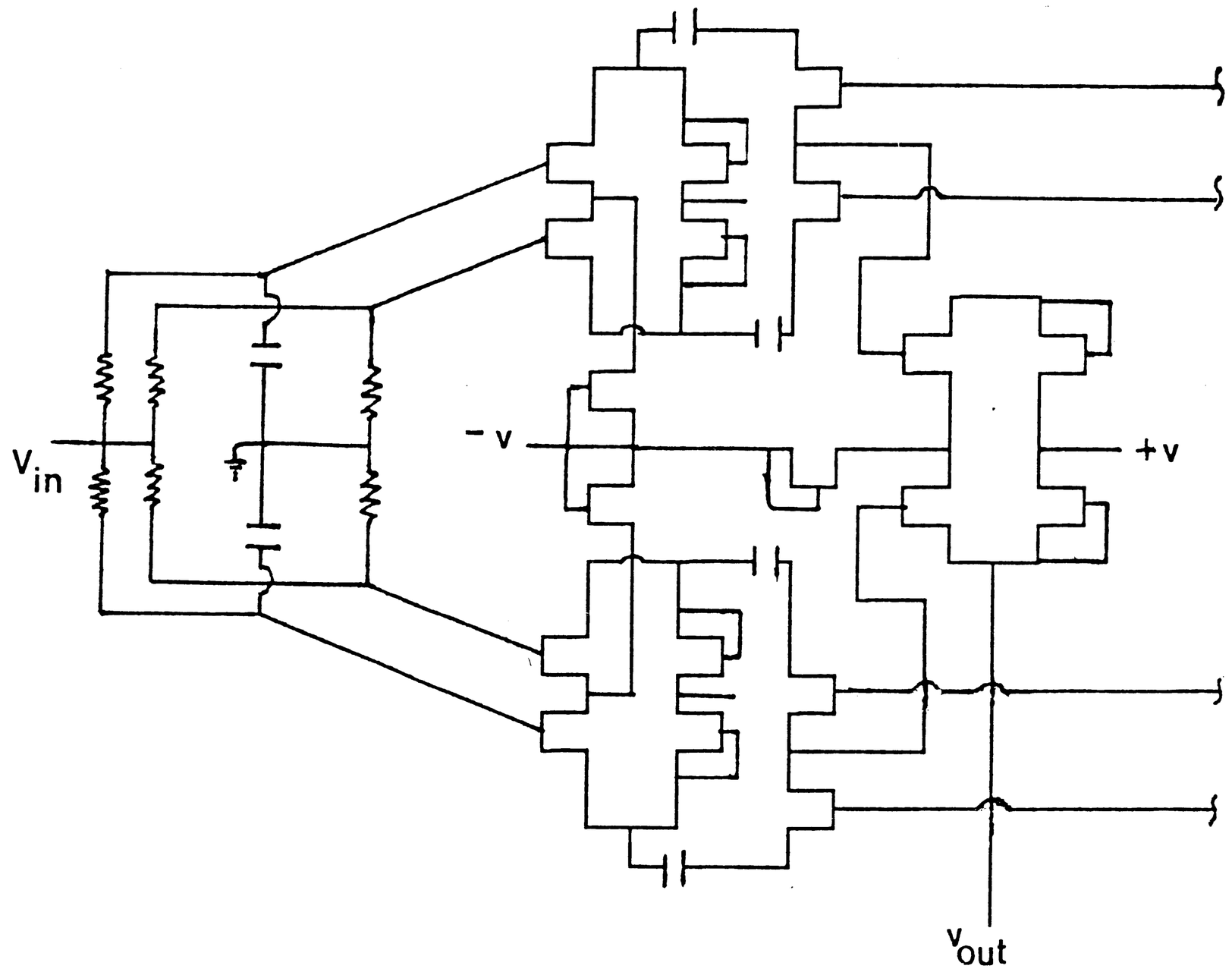


Fig. 28

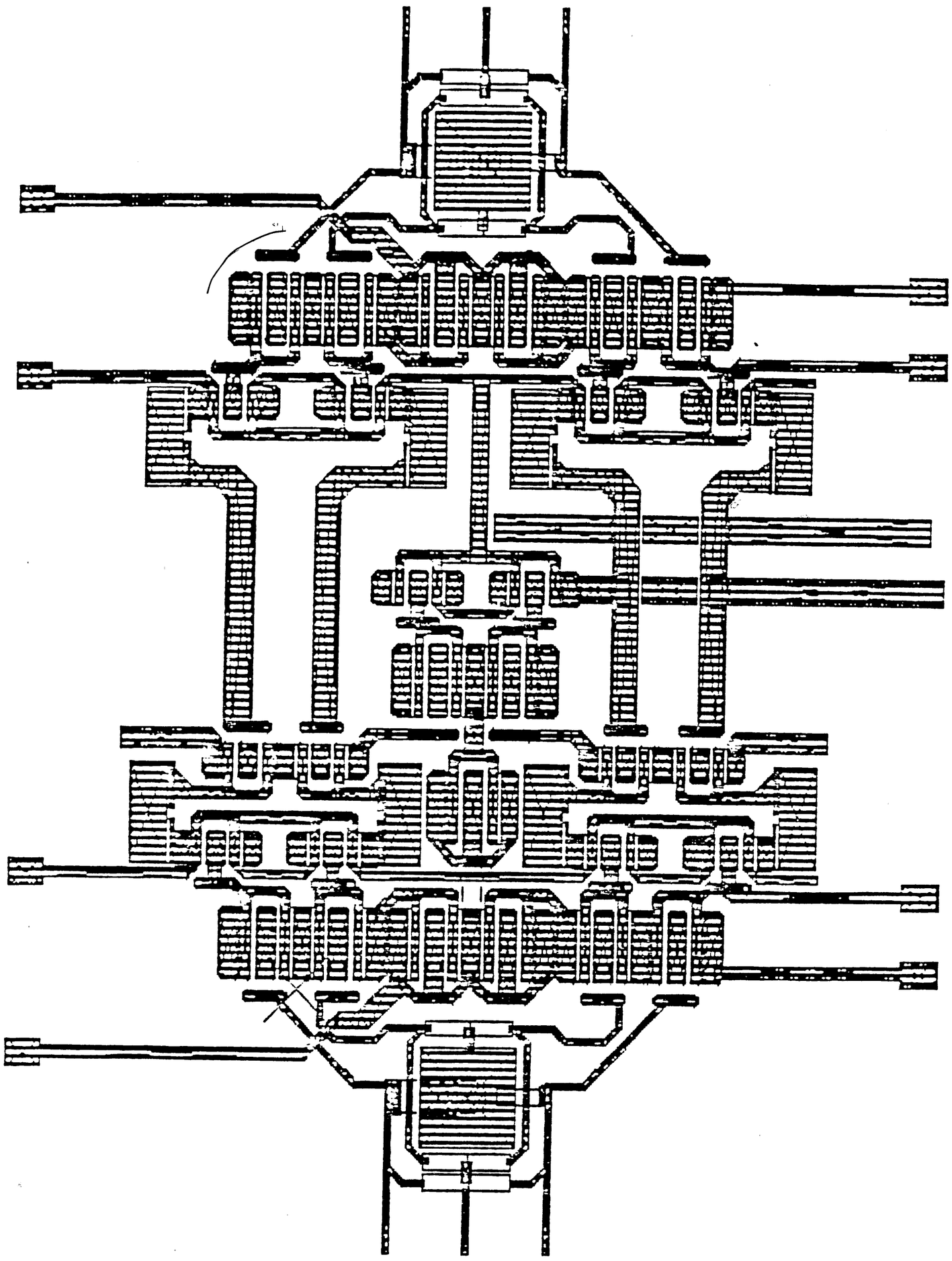


Fig. 29

Coupling is another problem with MMICs. The coupling is due to short distances between lines with different signals. In the serrodyne layout we have separated the antiphase signals by about half a substrate. This distance should be sufficient for avoiding coupling of the two outputs of the differential amplifier.

The allpass networks layed out well in the monolithic design implementation. First, the values of resistors and capacitors used are very easily implemented monolithically. The size of the components used in the allpass networks is small. The values of capacitors, for 50 ohm resistors, are 1pf and .165pf. These values of capacitance correspond to square capacitors with a side of 59.6um and 24.6um, respectively. Another beneficial aspect about the allpass networks is that the phase relation between the two networks should stay the same even if we encounter some additional resistance from the transmission lines. The reason for this is the phase relationship is determined by the RC constant of the allpass filters. Thus, changes in the RC constants may shift the center of the frequency bandwidth, however the phase relation between the two allpass filters should stay at 90 degrees.

The allpass networks are shown up close in figure 30. Three transmission lines which go toward the allpass filters can be seen. The center line is the input signal

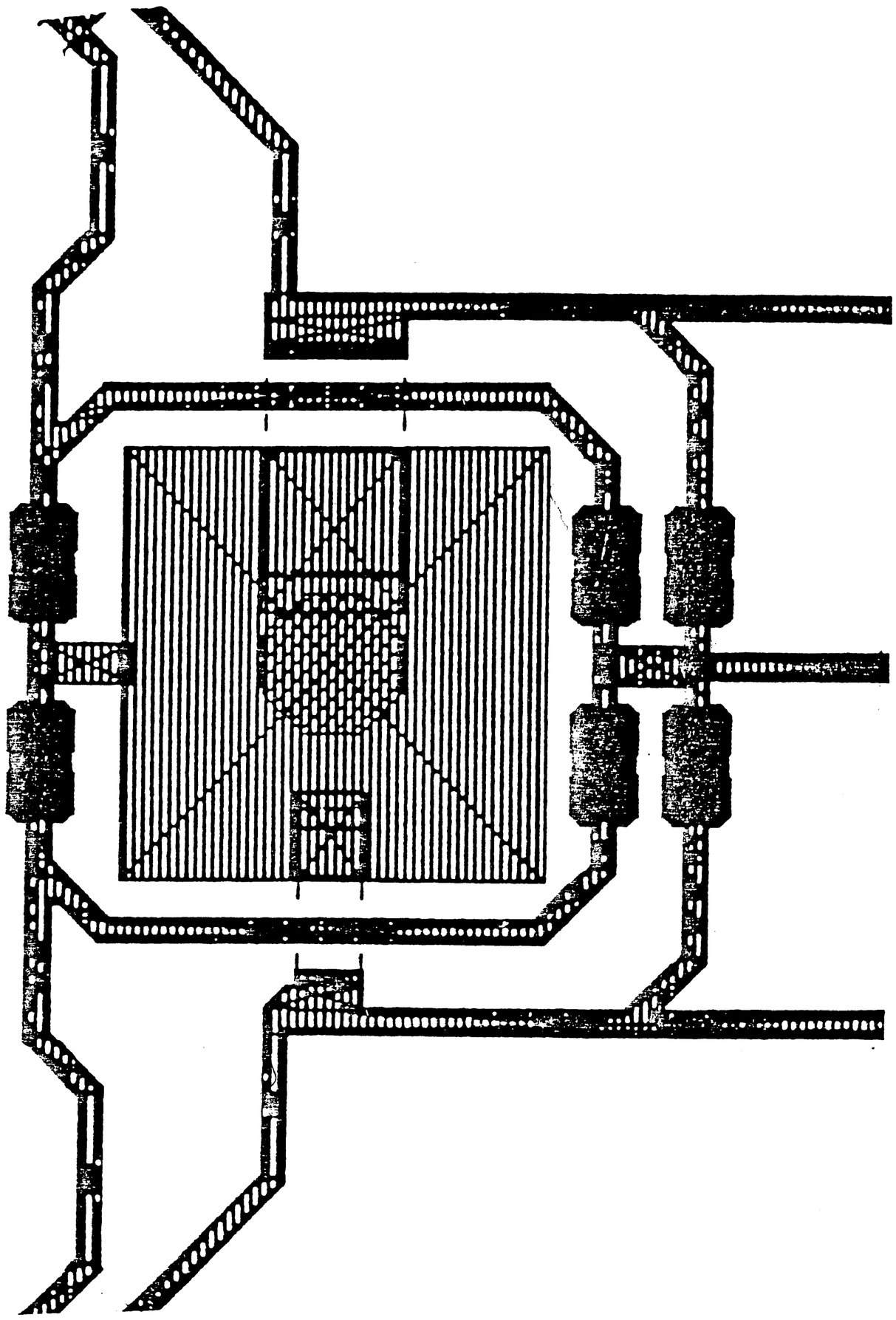


Fig. 30

or modulating signal depending on which side we are looking at. The two outer lines can be used to tune the values of capacitance or change the band of operation by changing the RC constants of the allpass networks.

MIXER LAYOUT

The mixer circuit in figure 31 consists of the MESFETs with the neccesary interconnects. The R.F., L.O., and I.F. signals will be coupled in when the circuit is being tested. The only disadvantages to this layout are the necessary cross overs which means we might see more R.F. or L.O. than expected in the ideal case.

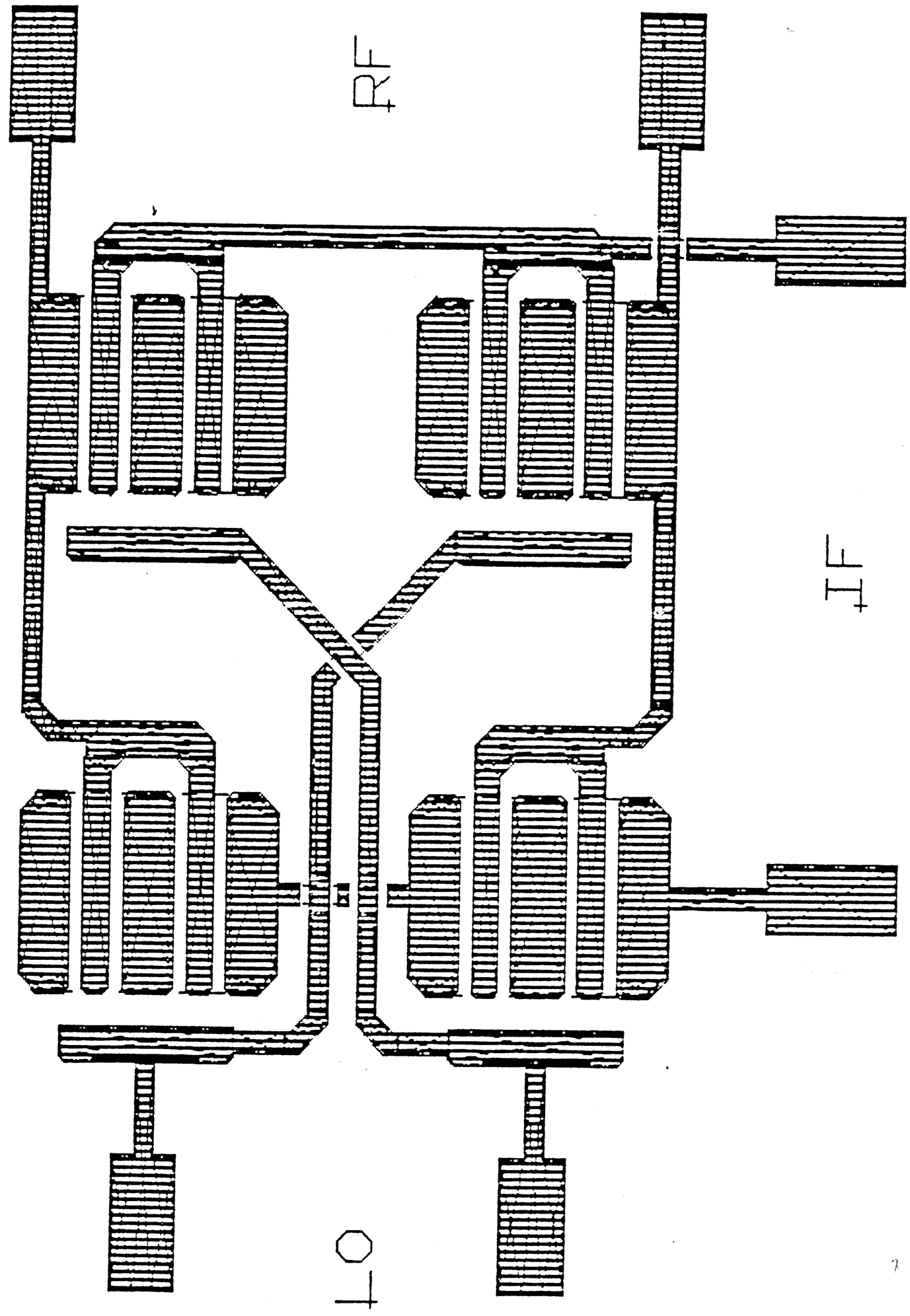


Fig. 31

REFERENCES

1 D. R. Decker, VLSI Electronics Microstructure Science, Vol. 11, New York Academic Press, 1985, ch. 3.

2 H. Statz et al.,"GaAs FET Devices and Circuit Simulation in SPICE", Raytheon Research Division, Lexington, Mass. 1985.

3 Asher Madiar, "A Fully AC Large-Signal Model of the GaAs MESFET for Nonlinear Network Analysis", IEEE MTT, vol. 36 no.1 1988.

4 Robert A. Pucel, "Performance of GaAs MESFET Mixers at X Band", IEEE MTT, vol. 24 p351-360, June 1976.

5 Rowan Gilmore, "Nonlinear Circuit Design Using the Modified Harmonic Balance Algorithm", IEEE MTT vol. no. 12 Dec. 1986 p. 1295

6 Erik L. Kollberg, "Microwave and Millimeter-Wave Mixers", IEEE Press 1984, New York, p341.

7 P. Bura and R. Dikshit, "FET Mixers for Communication Satellite Transponders", IEEE MTT-s,1976 p90-92.

APPENDIX A

VALUES OF C1 AND C2:

The phase of the allpass networks behaves as follows:

$$\theta = \tan^{-1}[-2\omega RC/(1-(\omega RC)^2)]$$

We want solve for θ = 45 and 135 degrees at the center of the band, 8GHz.

For θ = 45 degrees, $\tan\theta$=1 which gives the following;

$$1 = -2\omega RC1/(1-(\omega RC1)^2)$$

this gives C1=.96058505pf.

For θ = 135 degrees, $\tan\theta$=-1 which when solved for C2 at 8GHz gives C2=.16481033pf.

APPENDIX B

```
100 W=6E+09-2E+08
150 R=W
200 W=W*2*3.141592654#
300 W=W+2*3.141592654#*(2E+08)
350 R=R+2E+08
400 A=50*9.60585E-13*W
500 B=50*1.6481E-13*W
600 C=-2*A/(1-A^2)
700 D=-2*B/(1-B^2)
800 E=180*ATN(C)/3.141592654#
900 F=180*ATN(D)/3.141592654#
1000 G=E-F
1100 PRINT G E F R
1200 IF(R>1E+10) THEN END ELSE GOTO 300
Ok
RUN
 92.33821   57.82241 -34.51581   6E+09
 91.84106   56.24626 -35.5948   6.2E+09
 91.41458   54.74726 -36.66731   6.4E+09
 91.05358   53.32036 -37.73322   6.6E+09
 90.75326   51.96089 -38.79237   6.8E+09
 90.50922   50.66453 -39.84469   7E+09
 90.31736   49.42732 -40.89005   7.2E+09
 90.17388   48.24554 -41.92834   7.4E+09
 90.07526   47.11579 -42.95948   7.6E+09
 90.01828   46.03492 -43.98337   7.8E+09
 89.99992   45.00001 -44.99991   8E+09
 90.01739   44.00834 -46.00905   8.2E+09
 90.06809   43.0574 -47.0107  8.4E+09
 90.14762   42.14485 -48.00478   8.600001E+09
 90.25977   41.26852 -48.99124   8.8E+09
 90.39642   40.4264 -49.97003   8.999999E+09
 90.55768   39.6166 -50.94108   9.199999E+09
 90.74173   38.83737 -51.90436   9.399999E+09
 90.94693   38.0871 -52.85983   9.599998E+09
 91.17168   37.36425 -53.80743   9.799998E+09
 91.41455   36.66739 -54.74716   9.999997E+09
 91.67416   35.99521 -55.67897   1.02E+10
Ok
```

APPENDIX C

PHYSICAL DESIGN CONSTANTS:

RESISTORS

N = 500 ohms/square

N+ = 100 ohms/square

CAPACITORS

Co(sheet capacitance)	= 272 pf/sq. mm
Std. Dev. of Co	= 5% of Co

SPIRAL INDUCTORS

Current limits

1st Metal Cross-Under	= 2.8 ma/um of width
2nd Metal Cross-Over	= 4.0 ma/um of width
1st + 2nd Metal	= 6.8 ma/um of width

TRANSMISSION LINES

Current limits

1st Metal Only	= 2.8 ma/um of width
2nd Metal Only	= 4.0 ma/um of width
1st + 2nd Metal	= 6.8 ma/um of width
Relative Dielectric	= 12.9
Substrate Height	= 125 um
Loss Tangent	= .0001

APPENDIX C

PHYSICAL DESIGN CONSTANTS:

Substrate Height Var.	= 12.5 um
Line Width Variation	= 0.25 um
1st Metal Thickness	= 1.4 um
2nd Metal Thickness	= 2.0 um
Resistivity of Gold	= .0244 ohm-um

APPENDIX D

R AND C DIMENSIONS:

For C1 = .960585pf;

$$(272pf/mm^2)(x^2mm^2) = .960585pf$$

thus, $x = 59.5um.$

For C2 = .16481pf;

$$(272pf/mm^2)(x^2mm^2) = .16481pf$$

thus, $x = 24.5um.$

For 50 ohm N+ resistors;

W = 30um and L = 11.25um thus

$$R = 100 \quad (L + 3.8um)/W = 50.1667$$

VITA

R. Brian Khabbaz was born in Bethlehem, Pennsylvania on June 20, 1964. He graduated from Bethlehem Catholic High School in May 1982. He attended Lehigh University from August 1982 to June 1986 when he received a Bachelor of Science degree in Electrical Engineering with a minor in Applied Mathematics. Since August 1985, he has attended graduate school at Lehigh University where he has been a Research Assistant in the Computer Science and Electrical Engineering Department. His main research interests lie in the areas of microwave circuit design and analysis, electrooptics, and medical applications of microwave technology. Mr. Khabbaz is a student member of the IEEE.